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CZECHOSLOVAKIAN ACADEMY OF SCIENCES

Laboratory for Mathematical Machines

MACHINES FOR PROCESSING INFORMATION

Vol. II

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MACHINES FOR PROCESSING INFORMATION

Vol. II

MATHEMATICAL MACHINES

Czechoslovakian Automatic Computer SAPO

Statistical Analyzer

METHODS OF AUTOMATIC COMPUTING

Instruction Network

Solution of Systems of Linear Equations

Solution of Partial Equations

Interpolation with Punched Calculation

THEORY OF MATHEMATICAL MACHINES

Synthesis of Relay Circuits

Synthesis of Joint Mechanisms

Electronic Computing Circuits

Relays for Mathematical Machines

Addition of 2n Poles

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Setting up Instruction Nets from Prepared Units, Edited by Engr. Jan Oblonsky

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Instruction Nets for Transformation of Numbers in the Automatic Calculater SAPO, Edited by Engr. Jan Oblonsky

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PREFACE

The purpose of the present volume is to acquaint a wide public with the new results of the investigations in the field for machines for processing information. It contains the papers of the Collective of the Laboratory for Mathematical Machines and some outside reports. The majority of these papers was presented to the Second All-State Working Conference in the House of Science by the researcher J.E.Purkyne in December 1953 and to the Fifth Working Conference of the Laboratory.

The papers can be divided into three groups.

The first group contains descriptions of completed projects of mathematical machines, particularly of the Czechoslovakian automatic computer SAPO. The logical design of its memories, controls, and operational units is explained.

The papers of the second group relate to methods for the solution of problems on the automatic computer. These methods differ fundamentally from the usual numerical methods of calculation in that the use of arithmetic and nonarithmetical operations is not limited by the necessity of economizing on calculating operations, and depends on the special characteristics of the machine used.

Two types of machines to which the methods described in these articles relate are the Czechoslovakian automatic computer SAPO and the calculating perforator, which belongs to the new serially-produced Czechoslovakian machines for punched cards.

The third group comprises papers of the theoretical department (synthesis of relay circuits, synthesis of joint mechanisms, synthesis of 2n poles), and of the physical-technical department (electronic computing circuits, electromagnetic r

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lays).

The majority of the articles of the first two groups supplement the publication "Machines for Processing Information, Vol. I, Mathematical Machines", Prague, 1953, which contains an introduction to automatic computation, the codes of the Czechoslovakian computer SAPO, the fundamentals for the preparation of problems for calculation on the automatic computer, and an introduction to the working methods with machines for punched cards.

The authors thank Dr. V.Hruska for his conscientious scientific criticism. They also thank M.Sterbov for his collaboration in the preparation of the manuscript of H.Snelerov and his conscientious criticism of the majority of illustrations.

Council of Editors of the Laboratory for Mathematical Machines

Prague, 24 March 1954

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MACHINES FOR PROCESSING INFORMATION

1. Introduction

1.1 Automatic Computer SAPO. The Czechoslovakian automatic computer SAPO is a relay computer with a magnetic drum memory, with a capacity of 1024 words composed of 32 binary numbers (0 or 1). For working in the binary system floating points are provided*. The coding has been described in detail in another report (Bibl.1). Input and output proceeds by perforated cards. The entire machine contains about 7000 relays and 400 electron tubes. The computer is so designed that accidental errors occurring in any part of the machine have no influence on the accuracy of the result. The design of the automatic computer SAPO is the work of the collective of the Laboratory for Mathematical Machines of the Czechoslovakian Academy of Sciences. The creator of the basic design is A.Svoboda.

The automatic computer SAPO is composed essentially of three main parts. These are: the internal memory, the operational unit, and the control. The central memory stores the instructions according to which the machine calculates, the numerical information constituting the initial information for the solution of a given problem, the intermediate results obtained in the calculation, and the final results, registered at the end of the calculation, as well as the solution of the given problem. The operational unit receives from the memory the variables (words), carries out the prescribed operations, and returns the result to the memory. The control governs the course of the entire calculation, according to the instructions taken from the memory.

1.2. Words. As fully explained in another report (Bibl.1), the automatic com-

* The point is the symbol separating the negative from the positive digits (in any numerical system). In the decimal system, this is usually the decimal point.

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puter processes information in the form of words. The words may be numbers, or parts of instructions, or logical numerical symbols. The words are stored in the memory of the computer at locations known as addresses. Each address stores one word. Some instructions are composed of two words, which are always stored in the memory at two successive addresses, for example, the first word at the address p and the second word at the address p + 1.

1.3. Instructions. Each instruction contains five addresses, denoted by i, j, k, r, s, and the operational marks f_1 and f_2. The first word of the instruction contains k, r, f_1, and the second j, s, f_2, i. The addresses i and j are used when the word stored in the memory according to which the operation is to be carried out is prescribed by the mark f_1. The address k is used when the result of the executed operation is to be stored. The addresses k and s are used when the first words of two instructions are stored, one of which will control the computer in the next operation. Selection between them is done by the sign of the result of the executed operation, in such a way that, for a positive result, the instruction whose first part is stored at the address r is valid, and, for a negative result, the instruction whose first part is stored at the address s is valid. The operational mark f_2 controls the action of the input and output units of the machine. The form of the instructions has been fully described previously (Bibl.1).

1.4. Simple Scheme. The fundamental action of the automatic computer will be described on the basis of the greatly simplified scheme in Fig.1.1, taken the previous report (Bibl.1). This block diagram shows the control, the memory, and the operational unit. The track of the whole word is designated by double lines and the track of the dominator by simple lines. The track of the dominator dominates the replacement. The work of the machine passes through an interval of time, which is called the working cycle. In one working cycle, the machine carries out one instruction. First, <i> and <j>* stored, at those locations and sent to the operation-

* Here, <i> denotes the word stored in the central memory at the address i.

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al unit are selected from the internal memory at the addresses i and j. At the same time the operational unit is fed with the mark f_1, which specifies how the operation with the words <i> and <j> is to be carried out. Then, the next words are selected from the internal memory, stored at the addresses r, r + 1, s and s + 1. From these words two instructions are composed, one of which will control the machine in the next cycle. In the meantime, the prescribed operation proceeds in the operational unit. The result of this operation <k> is stored by the machine in the memory at the address k and, according to the sign, from the prepared two instructions the one which is to control the next cycle is selected. This completes one working cycle. The course of the next cycle is exactly the same, being controlled by the selected new instruction.

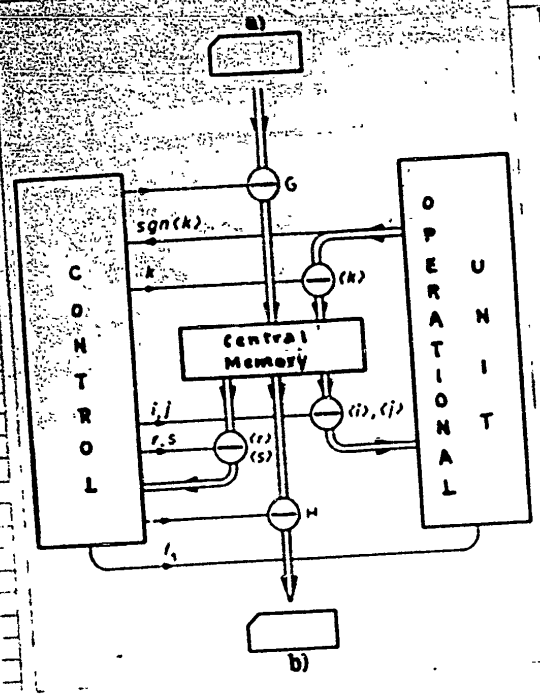

Fig.1.1 – Reading Scheme of Automatic Computer SAPO

a) input; b) output

The expected speed of the machine is about 10,000 cycles per hour.

Besides the described sectors of the cycle, the control also governs the input and output units with the switches, denoted by the letters G and H in Fig.1.1. The action of these units is determined by the mark f_2. In the following, both units will be considered parts of the control.

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1.5. Reliability of Operation. All actions of the control and the memory are verified by the control. For ensuring correctness of all executed operations, the operational unit is subdivided into three parts. It is composed of three wholly-identical operational units independent of each other. All three units carry out identical operations, including the announcing arrangement in the control, the so-called verifier, select the correct result, even if one of the units makes a mistake. One of the assumptions here is that two units will not make the same mistake at the same instant. The probability of such a simultaneous occurrence of two errors, however, is so remote that it is wholly negligible in practice.

On detecting any error, the control is able to prevent this error from influencing the accuracy of the entire calculation. This occurs automatically, without disturbing the calculation and without stopping the machine. The verifying circuits are designed in such a way that they verify their own action. The machine is wholly proof against the occurrence of the same error in the same instant in the same part. In the circuits of the control and memory where the probability of simultaneous occurrence of more than one error is greater, the verification is supplemented in such a way that it catches all errors.

Every detected error is automatically recorded. Thus a record is kept, showing the "state of health" of the entire computer. This enables early correction of defects, even before they manifest themselves in the form of errors. It is expected that these provisions will contribute to smooth operation of the automatic computer.

2. Internal Memory

Jindrich M. Marek

Received: November 20, 1953

Introduction

The calculation values, the various constants and the individual instructions of the network are set in the internal magnetic memory before beginning the calcula-

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tion. During the calculation, the control selects in succession from the internal memory the instructions and numerical values necessary for control and execution of

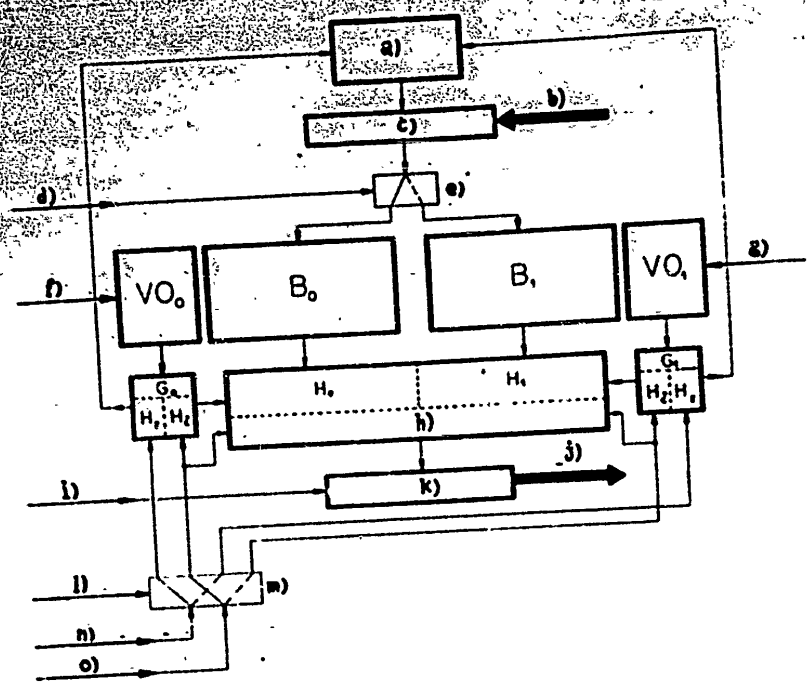

Fig.2.1 - Simplified Group Scheme of Internal Memory

a) Recording amplifier; b) Input; c) Input memory; d) Address of 9th row; e) Switch V1; f) Addresses of 0-8th rows; g) Addresses of 0-8th rows; h) Reading amplifier; i) Output impulse; j) Output; k) Output memory; l) Address of 9th row; m) Switch V2; n) Recording 0.1; o) Reading opening 1

the individual calculation steps (operations) and returns the results of the individual steps (intermediate results) to the internal memory. The internal memory has 1024 memory locations, which are assigned to the numbers 0 to 1023, the so-called addresses. Each memory location must be given one word (number or half of one instruc-

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tion) containing 32 binary digits 0 or 1 (in the binary system the mark 1 is used for unity).

A simplified group scheme is represented in Fig.2.1, and a more detailed scheme in Fig.2.2. The internal memory contains:

1. An input memory.
2. Two magnetic drums B_0 and B_1, each of which has 512 memory locations.
3. Two selective circuits VO_0 and VO_1 (which are provided with switches V1 and V2).
4. Two generators of starting pulses G_0 and G_1, dominated by the selective circuits.
5. A recording amplifier, which transforms the starting pulse into the corresponding recording pulse.
6. A reading pulse which, at the corresponding moment, transforms the read signal into a pulse which feeds the read word to the output memory.
7. An output memory.

2.1. Storage of Words in Internal Memory. The word to be stored in the internal memory enters from the control into the input memory, from where it is, at the corresponding moment, transferred by the recording pulse to the memory location determined by the address. Both of the circuits VO_0 and VO_1 and both of the switches V1 and V2 are set according to the address received from the control. In the interval of time when the recording on the magnetic drum is being carried out, the control feeds the recording pulse via the switch V2 to one of the two generators of starting pulses G_0 or G_1. Then, after a certain delay, the trigger pulse opens the switch H_2 of the starting pulse generator. During the open pulse, all 1024 of the memory locations of both rotating magnetic drums B_0 and B_1 pass in succession below the electromagnetic heads. The selective circuits VO_0 and VO_1 carry out, according to the address, the selection of one of the 1024 memory locations in such a way that, at the instant at which the given memory location is just passing below the electro-

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magnetic head, a signal is sent to the starting pulse generators G_o and G_1. The generator whose switch H has just been tripped feeds the starting recording pulse to the recording amplifier. In the recording amplifier, a short recording pulse is generated on arrival of the starting pulse, which transfers the word stored in the input memory via the switch V_1 to the magnetic drum B_o or B_1 and from there to the memory location of the given address.

2.2. Reading Words from Internal Memory. On reading the word from the internal memory, both selective circuits VO_o and VO_1 and the switch V_2 are set according to the address fed from the control. The read trigger pulse, according to the address, is fed from the control via the switch V_2 to the starting pulse generators G_o or G_1. The open pulse trips the reading switch H_{ch} in the corresponding starting pulse generator. Both the rotating magnetic drums B_o and B_1 continuously, induce in the reading windings of the electromagnetic heads, electric signals corresponding to the recording being carried out at the 512 memory locations of each of the drums. These signals are fed from the heads of the drum B_o to the switch H_o of the reading amplifier and from the heads of the drum B_1 to the switch H_1.

At the instant at which the memory location of the address set in the selective circuit passes below the electromagnetic head, the selective circuit sends a signal to the generators G_o and G_1. One of them passes through the open switch H_{ch} of one of the two generators to the corresponding switch H_o or H_1 of the reading amplifier. By opening the switch of the reading amplifier the read electric signal is transmitted to the amplifier. The amplifier transmits the read information to the input memory. Then, at the corresponding instant, the control transfers this information from the input memory to the starting pulse.

2.3. Input Memory. Before being stored in the magnetic memory, the word is intercepted in the input memory. The input memory contains 32 relays, which correspond to the 32 binary digits of the word. The untripped relays correspond to the digit 0, the tripped relays to the digit 1. Through one part of the contacts, these

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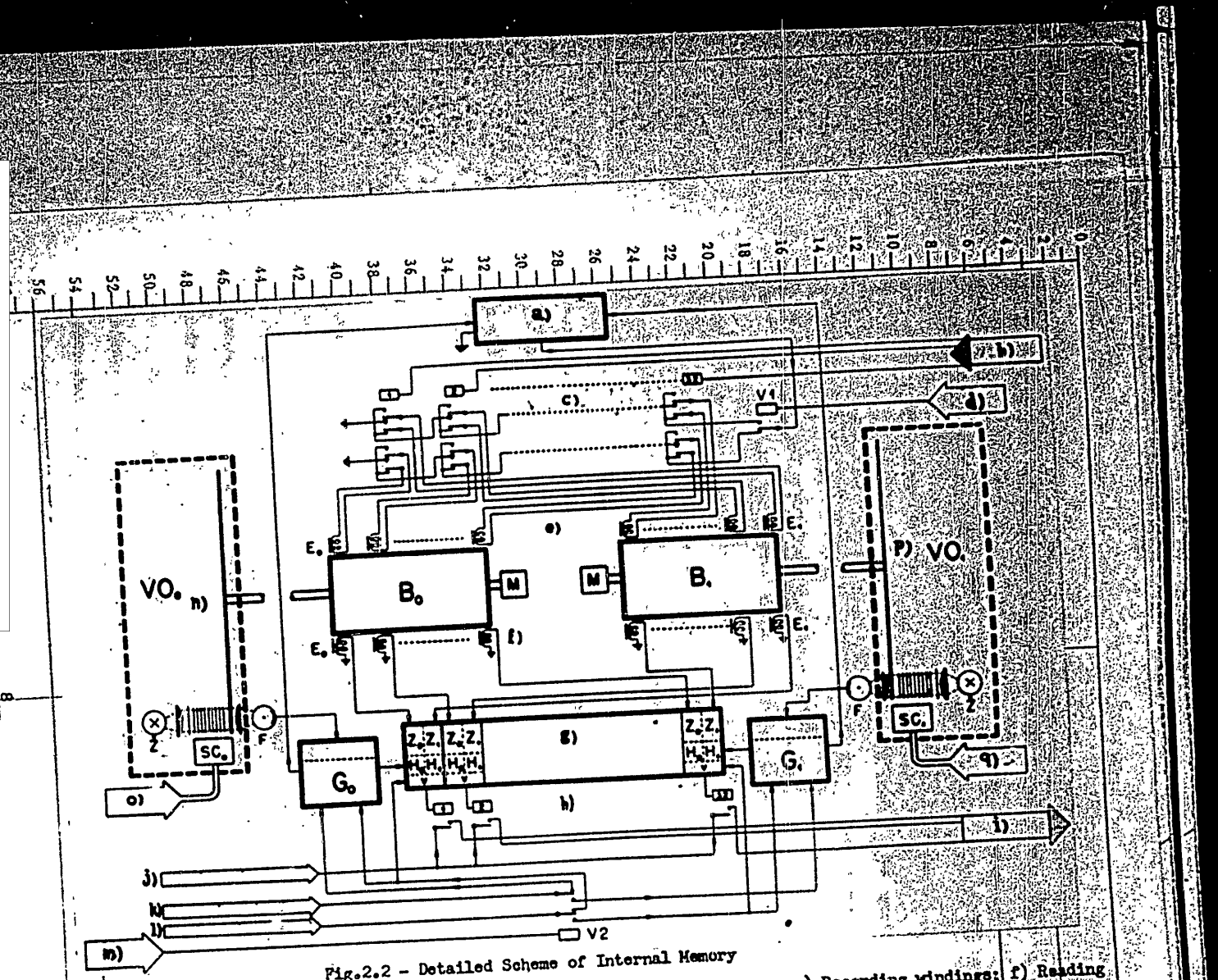

Fig.2.2 – Detailed Scheme of Internal Memory

a) Recording amplifier; b) Input; c) Input memory; d) 9th row of addresses; e) Recording windings; f) Reading windings; g) Reading amplifier; h) Output memory; i) Output; j) Output pulse; k) Recording trigger pulse; l) Reading trigger pulse; m) 9th row of addresses; n) Alignment of coil; o) 0th-8th rows of addresses; p) alignment of coil; q) 0th-8th rows of addresses

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32 relays are connected in series with the recording windings of the 32 electromagnetic heads E_0 of the magnetic drum B_0, and through the other part of the contacts with the windings of the heads E_1 of the drum B_1 (see Fig.2.2). The recording pulse passes through the windings connected at the contacts of the untripped relays in the one direction, and through the windings connected at the contacts of the tripped relays in the opposite direction. At this instant, the magnetic recordings depicting the words intercepted in the 32 relays of the input memory are formed at the surface of the corresponding magnetic drum.

2.4 Magnetic Drum. The magnetic drum is a metal cylinder coated on the outside with a thin ferromagnetic layer. Each drum is driven by its own motor. Close to the layer 32 electromagnetic heads are mounted which carry out the recording or reading of the 32 binary digits of the words. Each head on the surface corresponds to one recording track. Each recording track has 512 recording locations. To these recording locations, the numbers 0 to 511 on the one drum and the numbers 512 to 1023 on the other drum are assigned. To the recording locations for which there are 32 recording tracks for each drum, include the numbers which form one memory location. The assigned set of numbers is called the address of the memory location. It is clear that the recording locations which form one memory location, on rotation of the drum, pass below all 32 heads simultaneously. On rotating the drum, all memory locations pass in succession below the electromagnetic heads during one rotation. The heads are not arranged along a straight line of the surface, but are, for structural reasons, distributed around the drum. Each head has two windings: recording and reading. In Fig.2.2 the two kinds of windings are shown separately for the sake of legibility.

The ferromagnetic layer is premagnetized in one direction (Fig.2.3). The electromagnetic heads to carry out the recording in the same direction on this surface that is, in the direction of premagnetization, which corresponds to the digit 0, or in the opposite direction, which corresponds to the digit 1. On recording a new

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word it is not necessary to obliterate the old word first, since on recording of zero, an old permagnetised recorded unity proceeds in the direction of the premagnetization to the place where the new zero has to be. The direction of recording is reversed

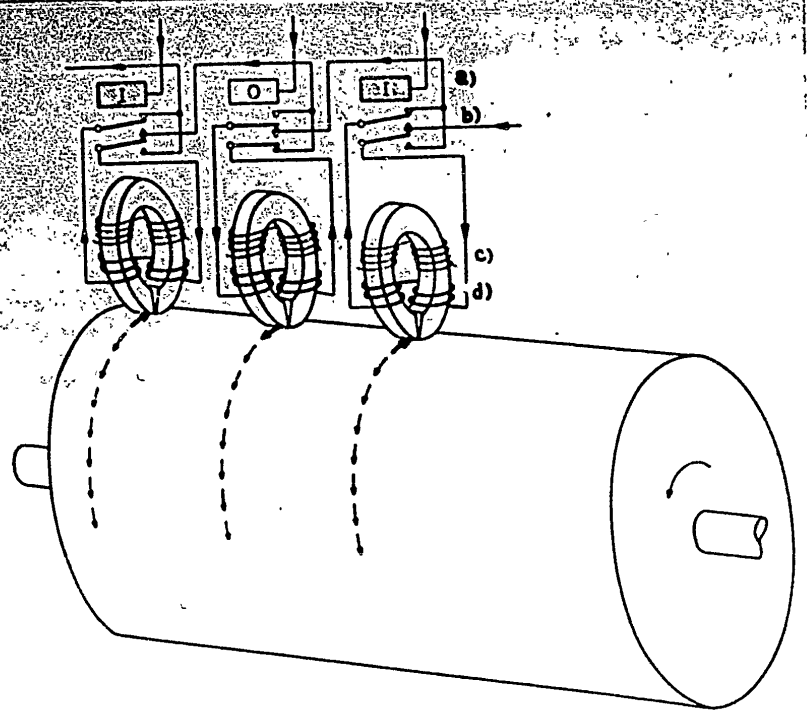

Fig.2.3 - Marking of Binary Digits on Premagnetized Layer of Drum

a) Input memory; b) Marking impulse; c) Reading winding; d) Recording winding

by commutation of the current in the recording windings of the heads. The commutation of the current in the individual heads is carried out by the relays of the input memory, according to the digits of the word to be stored in the magnetic memory.

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The selection of the corresponding memory location, at which the word is to be recorded or from which it is to be read, is carried out by the selective circuit according to the address arriving from the address distributor of the control.

2.5 Selective Circuit. The selective circuit is composed of an aligned coil, a principal diaphragm, a set of nine movable diaphragms, an optical system, pointers of diaphragms and a light source Z (see Fig.2.4). The aligned coil is permanently connected with the magnetic drum, where 32 holes of cross section about 1 mm^2 are provided. The openings are arranged so that the first opening is at a distance of 163 mm from the center of the coil and each of the succeeding holes is 1 mm farther from the center and forms an angle of $11^{\circ}15''$ (that is, $2\pi/32$) with the preceding one. The coil rotates before the fixed principal diaphragm. The model of the principal diaphragm forms 512 holes, giving 32 arc to 16 holes. Hereafter we shall speak of 32 rows and 16 columns of the principal diaphragm (see Fig.2.5). The rows are numbered from top to bottom with the numbers 0 to 31 and columns from left to right with the numbers 0 to 15.

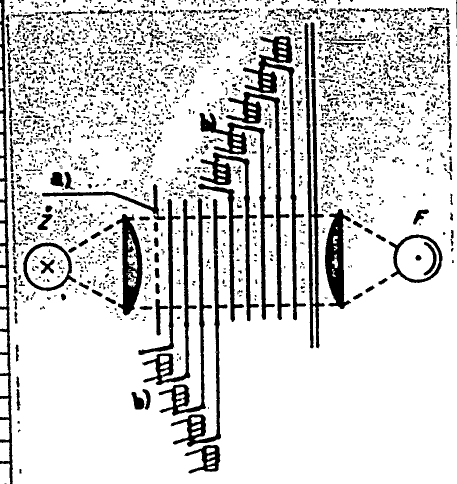

Fig.2.4 - Selective Circuit

a) Principal diaphragm;

b) Pointers of diaphragms

The principal diaphragm is located in the pencil of parallel light rays formed by the optical system. At each rotation of the ruled coil, each of the holes of the principal diaphragm becomes accessible in succession to the passage of light. There are 512 different places of the coil and hence also of the magnetic drum

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at which the 512 holes pass by in succession. Between the ruled coil and the principal diaphragm are interposed nine movable diaphragms controlled by nine two-

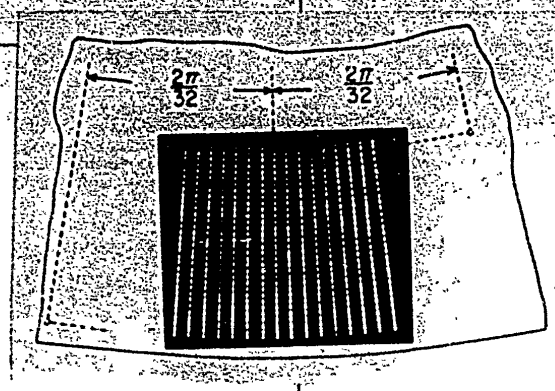

Fig.2.5 - Principal Diaphragm and Part of Ruled Coil

position electromagnets of the diaphragm pointers. Each of these diaphragms is provided with 512 holes. One half of the holes of each of the diaphragms in their fundamental position is covered by half of the openings of the principal diaphragm, while the other half of the holes in their attracted position is covered by the other half of the openings of the principal diaphragm. The araangement of the holes in each of the diaphragms is different and will be described later. According to the address sent from the distributor of addresses of the control, the electromagnets establish the corresponding combination of positions of the diaphragms. Only one of the 512 holes of the principal diaphragm is accessible to passage of the light, and with the help of the ruled coil one position of the magnetic drum is defined for the given addresses. Each diaphragm corresponds to one double row of numbers of the given address. The zero diaphragms up to the third row select the transmissibility of one of the 16 columns of the principal diaphragm. The pattern of the holes in one row of this diaphragm is the same for all 32 rows. It is therefore sufficient to describe only one row. In Fig.2.6 a segment perpendicular to the columns of the principal diaphragm and to the columns of the dia-

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phragms of the 0th to the 3rd rows is represented. The diaphragms are shown in the resting position, that is, the pointers of the electromagnets are not solicited. The parallel rays falling perpendicularly on the fixed principal diaphragm pass

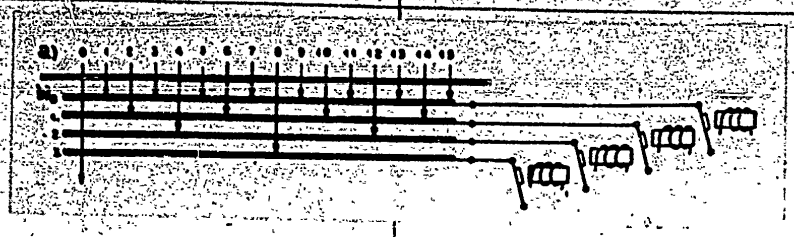

Fig.2.6 - Segment of Diaphragms of 0th to 3rd Rows in Fundamental Position

a) Row; b) Column

only through the 0 columns of the diaphragms.

Figure 2.7 represents the state in which the pointers of the electromagnets

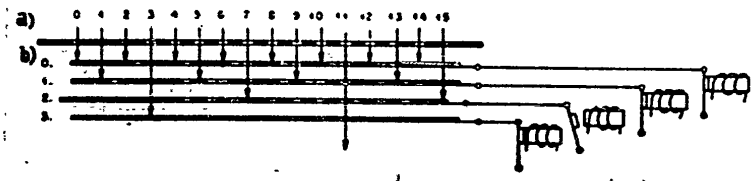

Fig.2.7 - Segment of Diaphragms of 0th to 3rd Rows. Diaphragms of 0th, 1st, and 3rd rows are attracted

of the 0th, 1st, and 3rd rows are solicited. The corresponding diaphragms are moved to the right by the diameter of the holes. There are now accessible to passage of the light the holes of the 11th column ($11 = 1.2^3 + 0.2^2 + 1.2^1 + 1.2^0 = 1011$).

The diaphragms of the 4th to the 8th rows (Fig.2.9) carry out the selection of one of the 32 rows of the principal diaphragm. The diaphragms of the 4th row

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are permeable to the even rows when present in the resting position, and to the odd rows when the pointers of the electromagnets are moved to the right by the diameter of the holes. The diaphragms of the 5th row are permeable in the fundamental

a)

b)		c)		d)		e)		f)	
g)	h)								
0		0		0		0		0	
	1	1		1		1		1	
2			2	2		2		2	
	3		3	3		3		3	
4		4			4	4		4	
	5	5			5	5		5	
6			6		6	6		6	
	7		7		7	7		7	
8		8		8			8	8	
	9	9		9			9	9	
10			10	10			10	10	
	11		11	11			11	11	
12		12			12		12	12	
	13	13			13		13	13	
14			14		14		14	14	
	15		15		15		15	15	
16		16		16		16			16
	17	17		17		17			17
18			18	18		18			18
	19		19	19		19			19
20		20			20	20			20
	21	21			21	21			21
22			22		22	22			22
	23		23		23	23			23
24		24		24			24		24
	25	25		25			25		25
26			26	26			26		26
	27		27	27			27		27
28		28			28		28		28
	29	29			29		29		29
30			30		30		30		30
	31		31		31		31		31

Fig.2.8 - Tabulation of Permeabilities of Rows of Principal Diaphragm and Those of 4th to 8th Rows

a) Rows of principal diaphragms permeated by diaphragms; b) 4th row; c) 5th row; d) 6th row; e) 7th row; f) 8th row; g) In fundamental position; h) In attracted position

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position to all 16 of the odd rows (that is, to the rows 0 and 1, 4 and 5, ..., 28 and 29), and in the attracted position to all 16 of the even rows (that is, to the rows 2 and 3, 6 and 7, ..., 30 and 31). The diaphragms of the 6th row are permeable in the fundamental position to all eight of the odd rows (that is, to the rows 0, 1, 2 and 3; 8, 9, 10, and 11; ...; 24, 25, 26, and 27), and in the attracted position to all eight of the even rows (that is, to the rows 4, 5, 6, and 7, 12, 13, 14 and 15; ...; 28, 29, 30 and 31). The diaphragms of the 7th row are in fundamental position permeable to the first and third of all four of the rows, and in the attracted position to the second and fourth of the four rows. The diaphragms of the 8th row will then be permeable to the first or second half of all of the rows. A tabulation of the permeability of the rows of the principal diaphragm and that of the diaphragms of the 4th to the 8th rows is presented in Fig.2.8. The arrangement of the diaphragms is shown in Fig.2.9 which shows only the boundary of the pencil of light rays passing through the principal diaphragm (0th row and 0th column). In this fundamental position of the diaphragms only the 0th row is permeable to the light. The other pencils of rays are intercepted by one of the five diaphragms, as can be seen from the ends of the arrows of the shown pencils of rays passing through the holes of the zero column of the principal diaphragm.

The combinations of positions of the small diaphragms of the 0th to the 3rd rows can therefore be selected only from the columns of the principal diaphragm, and the combinations of the small diaphragms of the 4th to the 8th rows only from the rows of the principal diaphragm. The combinations of positions of all nine of the small diaphragms can be selected from any of the 512 holes of the principal diaphragm in such a way that the holes are traversed by the pencils of the pencils of parallel rays which have traversed the same system of small diaphragms. The light flash which falls on the photocell upon the passage of one of the 32 holes of the lined coil by the pencil of rays determines the moment when the memory place of the corresponding combination of small diaphragms arrives below the jaw of the

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electromagnetic head.

2.6 Generator of Starting Pulses. The generator of starting pulses is composed of a photocell with a cathodic follower, of an amplifier, a recording switch and a

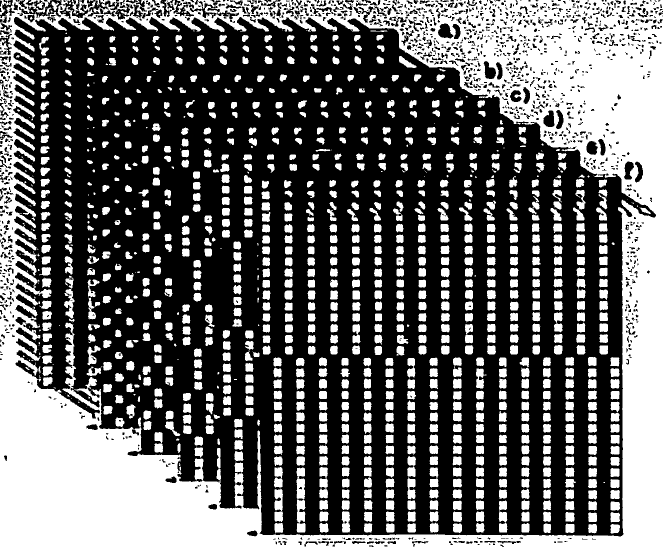

Fig.2.9 - Small Diaphragms of the 4th to the 8th Rows in the Fundamental Position

a) Principal diaphragm; b) Small diaphragms of the 4th row; c) Small diaphragms of the 5th row; d) Small diaphragms of the 6th row; e) Small diaphragms of the 7th row; f) Small diaphragms of the 8th row

reading switch (Fig.2.10). To each magnetic drum belongs one generator of starting pulses. The light signal which passes through the selective circuit established according to the address determines the instant when the address assigned to the memory place arrives below the electromagnetic head. In this instant the word stored at this memory place can be read, or a new recording carried out, in which

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case the original recording is simply "copied".

The light signal produces in the photocell circuit an electrical pulse. The latter is amplified by the three-step amplifier, and after derivation and repeated amplification is conducted to the recording and readying switches. From another input, the reading of the opening pulse goes from the control to the reading switch and the recording of the recording pulse to the recording switch. This opening pulse

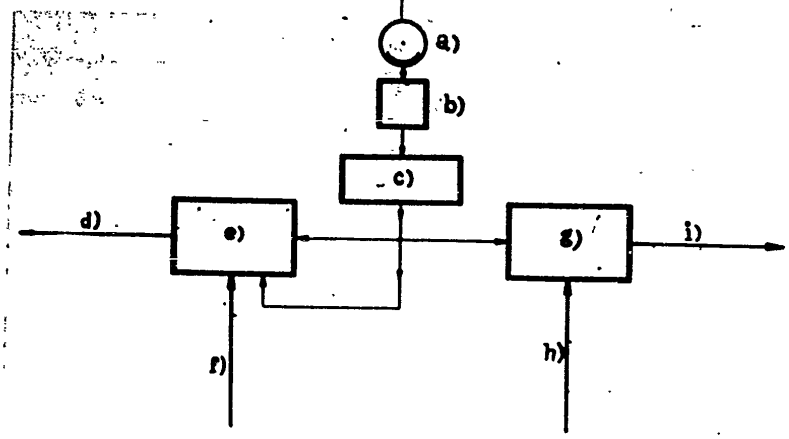

Fig.2.10 - Scheme of Generator of Starting Pulses

a) Photocell; b) Follower; c) Amplifier;

d) Starting recording pulse; e) Recording

switch; f) Opening and recording; g) Reading

switch; h) Opening and reading; i) Starting

reading pulse

determines the interval of time in which the reading or the recording occurs. Simultaneously with a photocell pulse and an opening pulse, a starting pulse occurs in the reading switch or in the recording switch. If the opening pulse is somewhat longer than the time of one rotation of the drum, it is possible while it lasts to generate the starting pulse corresponding to any of the 512 memory places. If,

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for the same memory place two starting pulses are generated, one in the beginning and one at the end of the opening pulse, this does not do any harm. For recording at a precisely-defined memory place, however, the opening pulse must arrive at the recording switch during the photocell pulse. Therefore, the arrival of the photocell pulse in the recording switch is delayed by a blocking pulse, which lasts somewhat longer than the active correction of the photocell pulse. This blocking only occurs in the absence of an opening pulse, and prevents arrival in the recording switch during the photocell pulse. If during this time there occurs in the switch the front of an opening recording pulse, a starting pulse is generated until the arrival of the next photocell pulse (after one rotation of the magnetic drum) toward the end of the opening pulse.

As already stated, two generators of starting pulses G_0 and G_1 belong to the central memory. The selection of the generator of starting pulses G_0 or G_1 and therewith the selection of one of the two drums for recording or reading is carried out by the router V2 according to the digits of the 9th row of the address.

2.7 Recording Amplifier. The signals are conducted to the common recording amplifier from the recording switches of the two generators of starting pulses. This eliminates the selection of the drum carried out by the router V2 for the recording. The recording amplifier contains a generator of recording pulses and a final amplifier. The starting pulse generates a very short recording pulse in the generator of recording pulses. The latter, after amplification in the final amplifier, is conducted to the router V1, which is actuated by the control according to the digits of the 9th double row of addresses prepared in the distributor of addresses (see Fig.2.2). Router V1 conducts the pulse via the contacts of the 32 relays of the input memory to the memory winding of either the head E_0 of the magnetic drum B_0 or the head E_1 of the drum B_1. A 32-place word in the relays of the input memory, is prepared for recording. The unsolicited relays corresponding to the digits 0, connect the recording winding with the recording circuit in such a way

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that the recording pulse passes through the ferromagnetic layer of the drum of the magnetic recorder in the same direction as the direction of the premagnetization. The solicited relays corresponding to the digits I, enable crossing of the lead-in windings and therewith of the recording in the opposite direction.

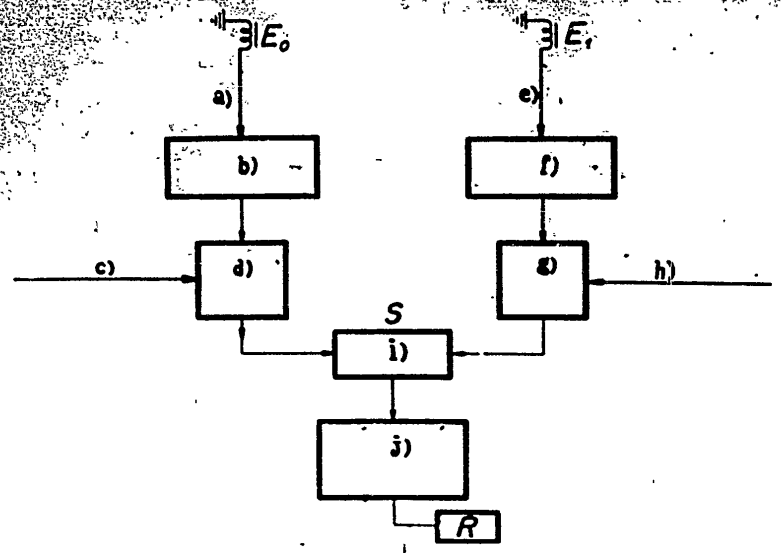

Fig.2.11 - Scheme of One of 32 Units of Reading Amplifier

a) Reading signal; b) Input amplifier Z_0; c) Reading Starting pulse; d) Switch H_0; e) Reading signal; f) Input amplifier Z_1; g) Switch H_1; h) Reading starting pulse; i) Mixer; j) Input amplifier VZ.

2.8 Reading Amplifier. The reading amplifier is composed of 32 units. Each binary digit of the word belongs to one electromagnetic head E_0 of the drum B_0, one electromagnetic head E_1 of the drum B_1, one unit of the reading amplifier and one relay R of the input memory. A unit of the reading amplifier contains (Fig.2.11) an input amplifier Z_0 and switch H_0 for the head E_0, an input amplifier Z_1 and

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switch H_1 for the head R_1, a mixer S and an input amplifier V2.

The magnetic recording in the ferromagnetic layer of the rotating drum induces intermittently in the reading windings of both electromagnetic heads an electrical signal (see Fig.2.12). The read signal is conducted from the heads to the corresponding amplifiers Z_0 and Z_1 and after amplification to the switches H_0 and H_1. At the next input the reading starting pulse is conducted either to the switch H_0 from the generator of starting pulses G_0, or to the switch H_1 from the generator G_1, (this is determined by the digits of 9th row of the address according to how they have been set by the router V2; see Fig.2.2). The starting pulse actuates one of the two switches at the simultaneous presence of an amplified read signal. The read signal given by either the switch H_0 or the switch H_1 is conducted by the mixer to the final amplifier. The bistable circuit in the amplifier causes the read signal to arrive in the input memory through the intermediary of the corresponding relay R.

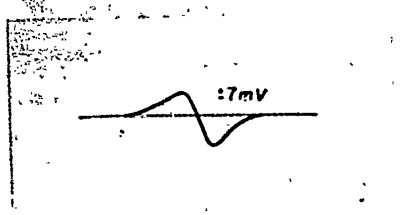

Fig.2.12 - Electrical Signal Occurring at Reading of Recorded Digit I

2.9 Output Memory. The output memory is composed of 32 relays. Each of these relays is connected with the anodic circuit of the final electronic tube belonging to the unit of the reading amplifier. In the output memory, the read word is intercepted at the moment it is sent to the control for further processing. Its transmission from the output memory is carried out by the output pulse.

The nullification of all of the relays occurs directly before the new reading, in such a way that the reading opening pulse sent out by the control to the generator of starting pulses also leads simultaneously to the bistable circuit of the final amplifiers of all 32 units, bringing all of the relays into the fundamental zero position.

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3. Control

Jan Oblonsky

Received: November 18, 1953

The control is the part of the automatic computer which governs the operation of the whole calculation according to the instructions which it takes from the central memory. It governs the selection of the word from the central memory, sends it to the operational unit, verifies the calculated result, and governs its storage in the central memory. The control also governs the input and output units of the computer, and adapts their functioning to all of the operations occurring in the computer.

The description of the control is divided into four parts. In the first part (paragraph 3.1) the whole scheme of the control is presented, to which is added a detailed description of the component parts of the control circuits. In the second part (paragraphs 3.2-3.8) a description of the action of the control of the operation of the machine is presented. First the governance of the calculation (paragraph 3.3) and the change of instructions (paragraph 3.4) is described. Then the functioning of the verifying device (paragraphs 3.5-3.7) is explained and finally, the method of automatic elimination of ascertained errors (paragraph 3.8). The third part (paragraphs 3.9-3.12) describes the action of the control and the input unit of the computer at the storage of information in the machine. The fourth part (paragraphs 3.14-3.17) describes the action of the control and the output unit at the output of information from the machine.

Scheme of Control

3.1 Scheme of Control. A simplified scheme of the control of the SAPO is presented in Fig.3.1. In it are shown the principal parts of the control, and the ~~parts of the computer governed by the control are indicated. The principal signal paths are indicated in double lines, the distances of which show how many binary~~

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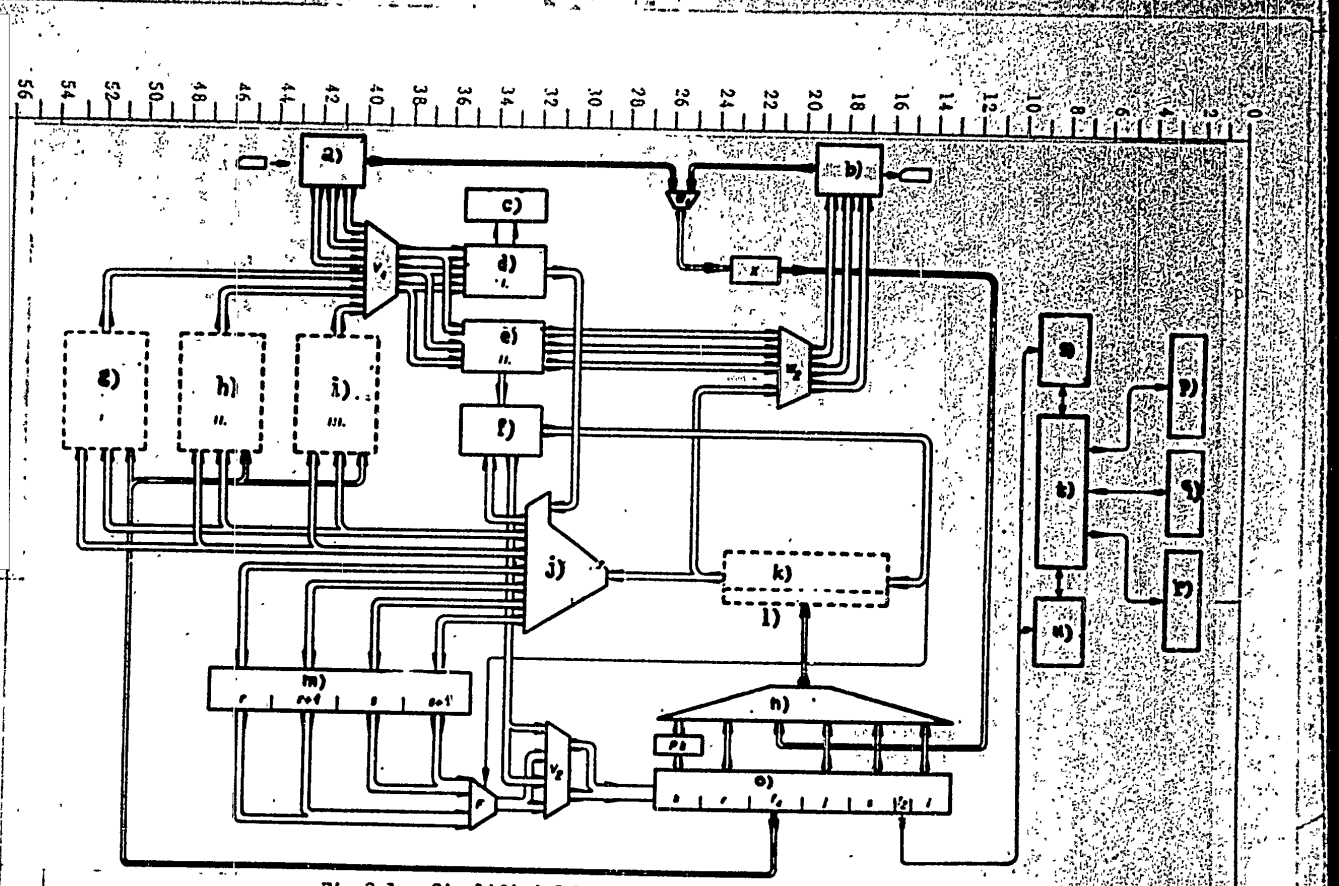

Fig.3.1 - Simplified Scheme of Control of SAPO

a) Input unit; b) Output unit; c) Adder of errors; d) Verifier I; e) Verifier II; f) Verifier III; g) Comparator; g) Operational unit I; h) Operational unit II; i) Operational unit III; j) Distributor of output memory; k) Central memory; l) Selective circuit; m) Preparatory instructional memory; n) Distributor of addresses; o) Governor of instructional memory; p) Printer of errors; q) Master table; r) Signal board; s) Master of output unit; t) Central master; u) Master of output unit

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digits belong to them, as well as their course. The dominating signal paths, when they are shown on the drawing, are indicated by simple lines. The majority of the units and the auxiliary memories of the control are shown separately, and the routers and distributors are depicted as trapeziums. The inputs are denoted by arrows directed toward the corresponding units, the outputs by arrows directed away from the units.

The Distributor of the Output Memory is a 32-path router with two inputs and seven outputs. All of the inputs and outputs are 32-path. The main input is connected with the central memory, while the secondary inputs are connected with the verifier I. Two outputs are connected with the operational unit, four further outputs are connected with the preparatory instructional memory. Seven outputs are connected with the comparator. The distributor of the output memory connects in succession operational unit, the prepared instructional memory and the comparator with the output central memory and thus intermediates the transmission of the words from the central memory to the respective units. Moreoever, at the corresponding moment the comparator is connected with the verifier I.

The Preparatory Instructional Memory (PIP) is an auxiliary relay memory composed of four partial memories, denoted by r, r + 1, s, s + 1. Each of these memories has a capacity of 32 double places. The outputs of these memories are connected with the distributor of the output memory, whose outputs are paired and connected with the functional router F. The PIP serves to compose two instructions from the words (5), (5 + 1), <s> and <s + 1> selected from the central memory and intercepted therein as they are to be used for the governance of the machine.

The Functional Router F is a 64-path router with two inputs and one output. The inputs of the router F are connected with the preparatory instructional memory, its output with the input of the router RIP. The router F selects two of the four output partial memories PIP and connects them with the input of the router RIP, thus carrying out the selection of one of the two instructions which will govern

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the machine in the next working cycle. The router F is governed by the recording place of the result of the operation just carried out.

The Input Router RIP (V_2) is a double 32-path router with two inputs and one output. The input, connected with the functional router F, and the output, connected with the governor of the instructional memory, have 64 signal paths, while the input, connected with the comparator, has 32 signal paths. The router serves to connect either all of the 64 places of the governor of the instructional memory with the functional router F or one or the other of its halves with the comparator.

The Governor of the Instructional Memory (RIP) is a relay memory with a capacity of 64 double places. It is divided into seven partial memories with various numbers of places. The memories denoted k, j and i are 10-place, the memories denoted r and s are 9-place, the memory f_1 is 12-place and the memory f_2 is 2-place. In all the governor of the instructional memory has one 64-path input connected with the input of the router RIP and seven outputs corresponding to the individual partial memories. The output memories r, j, s and i are connected with the distributor of addresses, the output memory k is connected with the address memory P_k, the output memory f_1 is connected with all of the operational units, and the output memory f_2 is connected with the master input unit and the master output unit. The governor of the instructional memory serves to intercept the instruction (that is, two words) which governs the whole calculation in the given working cycle. The individual addresses k, r, j, s, i and the operational marks F_1 and f_2 of the governor of the instructions are intercepted in the partial memories of the corresponding designations.

The Address Memory P_k is a 10-place relay memory. Its input is connected with the partial memory k of the governor of the instructional memory, its output is connected with the distributor of addresses. The address memory P_k intercepts the address k to change the content of the governor of the instructional memory. The purpose of this memory is explained in paragraph 3.8.

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The Distributor of Addresses is a 10-path router with six inputs and one output. Four of the inputs of the distributor of addresses are connected with the outputs of the partial memories r, j, s and i of the governor of the instructional memory. One of the inputs is connected with the address memory P_k and one with the address memory X. The output of the distributor of addresses is connected with the selective circuit of the central memory. The distributor of addresses is connected in succession with the partial memories of RIP containing the addresses, and the address memory P_k is, in the event of X, connected with the selective circuit of the central memory of the computer.

The Central Memory of the automatic calculator is a magnetic memory with a capacity of 1024 of 32 double places. It is described in Part 2. It has two inputs and one output. The output has 32 signal paths and is connected on the one hand with the distributor of the output memory and on the other hand with the router of the output unit W_2. The 32-path input is connected with the comparator, the 10-path input is connected with the distributor of addresses. In the central memory, the information obtained from the comparator is stored, and from it is sent the information to the distributor of the output memory, or eventually to the router of the output unit W_2. The places in the memory where this information is stored and the places from which it is sent out are determined by the selective circuit of the memory according to addresses furnished by the distributor of addresses.

Operational Units I, II and III are three absolutely-similar operational units as described in Part 4, each having three inputs and one output. Two of the 32-path outputs are connected with the distributor of the output memory. The 12-path input is connected with the partial memory f_1 of the governor of the instructional memory. The output of each of the operational units has 31 signal paths, and is connected with one of the inputs of the input router of the verifier. All three of the operational units carry out similarly but independently of each other operations on the words <i> and <j> from the distributor of the output memory according

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to the operational mark f_1 from the governor of the instructional memory and send the result <k> via the output router of the verifier to the verifiers I and II.

The input router of the verifier (V_1) is a triple 31-path router with two triple inputs and one triple output. One of the outputs is connected with the operational unit, the other with the input unit. The output is connected with verifiers I and II. The inputs of the router of the verifier connect the verifier with either the output of the operational unit or the input unit.

Verifier I contains three relay 31-place memories supplemented by an announcing circuit and a circuit for announcing errors. It has three 31-path inputs connected with the input of the router of the verifier, one 31-path output connected with the distributor of the output memory and one 93-path output connected with the adder of errors. In verifier I, the results obtained via the output router of the verifier from the operational unit are intercepted. It announces the verification of the result, which is then sent to the comparator. The ascertained error is announced by verifier I to the adder of errors.

Verifier II likewise contains three relay 31-place memories supplemented by an announcing circuit. All of its inputs and outputs have 31 signal paths. Three inputs are connected with the input router of the verifier, three outputs are connected with the router W_3 of the output unit. One output is connected with the comparator. In verifier II the results obtained via the input router of the verifier from the operational unit are intercepted. The result obtained is announced and sent to the comparator. Moreover, the verifier can send three intercepted results without change to the router of the output unit.

The adder of errors contains 93 relay memories for interception of the errors announced by the verifier, and a circuit for their evaluation and announcement to the central master.

The comparator contains two 32-place relay memories supplemented by a comparing circuit for producing the signals of the unity trials. The input connected with

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verifier II has 31 signal paths, the input connected with the distributor of the output memory has 32 signal paths. The output connected with the input router of the RIP and the output connected with the memory have likewise each 32 signal paths. In the comparator the results announced in the two verifiers are compared with each other. Moreover, the words sent to the central memory for storage are compared in it, with the word arriving immediately afterward from the memory for verification of the reading. Moreover, the signals of the unit trials (parties) are produced in the comparator. If necessary, the content of the comparator is sent to the input router of the RIP.

The input unit contains a device for feeding perforating cards and reading the information to be perforated in the cards. It has a total of four outputs. Three of them have 32 signal paths each, and are connected with the input routers of the verifiers. The fourth, with 11 paths, is connected with the address router W_1. The unit takes the information from the perforated cards and sends it via the input router of the verifier to the verifier and via the address router W_1 to the address memory X.

The Address Router W_1 is an 11-path router with two inputs and one output. One of the inputs is connected with the input unit, the other input is connected with the output unit. The output is connected with the address memory X. The address router W_1 connects the address memory X with either the input or the output unit.

The address memory X is an 11-place relay memory supplemented by a circuit for verification of the unity trials. It has an 11-step input connected with the address router W_1 and a 10-path output connected with the distributor of addresses. In this memory the addresses arriving from any of the units via the address router W_1 where they are verified, are intercepted and then sent via the distributor of addresses to the selective circuit of the central memory.

The output unit contains a device for feeding perforating cards, a device for reading the information to be perforated on the cards, and a perforator. It has

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three inputs each with 32 signal paths connected with router W_2 of the output unit and one 11-path output connected with the address router W_1. The unit takes the information from the perforated cards and perforates in the same cards further information obtained via router W_2 from either the central memory or verifier II.

The Router of the Output Unit (W_2) is a triple 32-path router. It has three inputs each with 31 signal paths connected with verifier II and one 32-path input connected with the central memory. Three outputs of 32 paths are connected with the output unit. In one position of router W_2 all three of the 32-path inputs of the output unit are connected with the 32-path output of the central memory. In the other position of router W_2, 31 paths of each of the three inputs of the input unit are connected with the corresponding outputs of verifier II.

The Master of the Input Unit is a device which takes over the function of the central master during the operation of the input unit. Its input is connected with the governor of the instructional memory. The master of the input unit also connects with domination the paths with all of the parts of the control which are in action during the operation of the output unit.

The central master is a device which dominates the control of the automatic computer. It also connects with domination the announcing signal paths with all of the parts of the control, with the master table, the signal board and the printer of errors. The central master starts and stops the machine, intermittently verifies the action, not only of the whole computer but also of itself, carries out measures directed toward preventing an influence of fortuitous and systematic errors on the correctness of the calculation, and makes announcements on the progress of the calculation and the condition of the computer.

The Signal Board signals the momentary condition of the machine. It is connected with the central master.

The Printer of Errors records fortuitous and systematic errors occurring in any part of the automatic computer. It produces permanent records of the condition

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of the computer, and facilitates the search for defects.

The master table is connected with the central master. The computer, the input unit and the output unit, are started and stopped from the master table and governed with auxiliary devices of the computer (generators, motor, danger sources, cooling, etc).

Action of Control

3.2 Introduction. The action of control proceeds in the working cycle, which is continuous during smooth operation of the machine. One working cycle is divided into 16 steps, numbers from 1 to 16. Each step is divided into two partial steps, denoted a and b. The working cycle, thus divided into 32 partial steps, forms a time scheme, during which all of the events occurring in the whole automatic computer proceed. For various reasons, which need not be explained here, the numbering of the steps is shifted in such a way that the working cycle begins at step 10b.

The action of control consists in certain events which follow each other in regular sequence of their own accord. For facilitating the understanding, however, the description of these individual events and their connections with each other will be postponed to paragraph 3.8, which describes the processing of information on errors.

For the description the simplified scheme of the corresponding circuits represented in Fig.3.1 will be used on the one hand, and on the other hand, the time diagram of the transmission of the information. An example of such a diagram is presented in Fig.3.3. The diagram is divided by vertical lines into 32 columns corresponding to the partial steps of the working cycle. The step numbers are given at the head of the diagram. Horizontal lines are assigned to the individual circuits, whose names are noted on the left of the diagram. The transmission of the information is denoted by heavy vertical lines. The circuits from which the information starts and the circuits in which it arrives are denoted at circles on the corresponding horizontal lines. The locations of these circles in the columns

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indicate the partial steps in which the transfer of the information is carried out. The directions of the transfers are indicated by arrows. With each of the transfers, the transferred information is also denoted along the corresponding line. If any information remains in a circuit for a certain length of time, and this must be indicated, this is done on the diagram by bending the vertical line to the horizontal line assigned to the given circuit, and prolonging it to the column corresponding to the partial step in which the information is either obliterated or transferred further.

3.3 Governance of the Calculation. The control governs the calculation in the automatic calculator by selecting the words from the central memory, storing them in the operational units, governing the operations in the operational units, and storing the results in the central memory according to the instructions likewise selected from the central memory. The instructions to govern the action of the working cycle next to be carried out, are stored in the governor of the instructional memory RIP.

The circuits for storing the variables in the operational units governing the operations and storing the results in the memories, are copied from Fig.3.1 in Fig.3.2. These are: the governor of the instructional memory RIP, the address memory P_k, the distributor of addresses, the distributor of the output memory, the input router of verifier V_1, verifier II and the comparator. Also indicated by dotted lines in Fig.3.2 are the three operational units and the central memory. The actions of the circuits are represented in Fig.3.3. The first (in the partial step 10b) goes from the partial memory f_1 of the governor of instructional memory RIP to all of the operational units of operational mark f_1, which determines what kind of operation will be carried out in this working cycle. Then the distributor of addresses connects with the memory the output of the partial memory RIP-j, and thus stores the address j arriving in the partial step 12b in the selective circuit of the central memory. Next the distributor of the output memory connect the

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of the central memory with the input "j" of all three operational units, and the word <j> selected according to the given address arrives in the partial step 15a in the operation units. In the meantime, the distributor of addresses has connected the central memory with the partial memory RIP-i, and thus stored the address <i>

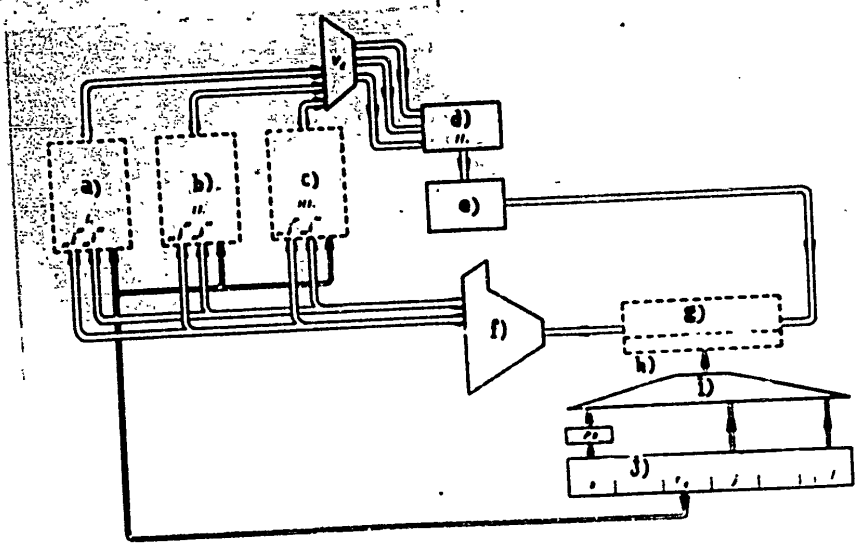

Fig.3.2 - Circuits for Storing Words in Operational Units, Governing Operations and Storing Results in Central Memory

a) Operational unit I; b) Operational unit II; c) Operational unit III; d) Verifier II; e) Comparator; f) Distributor of output memory; g) Central memory; h) Selective circuit; i) Distributor of addresses; j) Governor of instructional memory

arriving in the partial step 14b in the selective circuit of the memory. In the next partial step 1a the selected word <i> arrives in the input "i" of all of the operational units, which was previously connected with the distributor of the out-

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put of the memory.

In partial step 14b the address k arrives from RIP in the address memory P_k, where it is stored until the end of step 8. In this step the distributor of addresses is connected with the output of the address memory P_k, and thus stores the

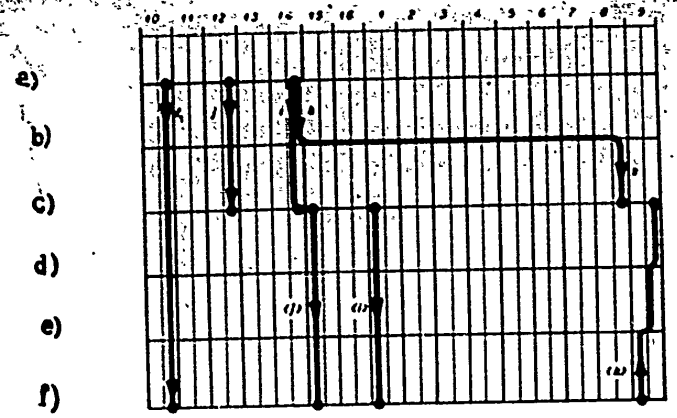

Fig.3.3 - Time Diagram of Actions of Circuits from Fig.3.2
a) RIP; b) Address memory P_k; c) Central memory; d) Comparator; e) Verifier II; f) Operational unit

address arriving in the selective circuit of the central memory (in the partial step 8b). In the meantime the corresponding operation has occurred in the operational unit, and the result has arrived in the verifier II in the partial step 9a. In the latter formed from the three results one result, which in the partial step 9b arrives in the comparator, and is stored in the memory at the given address.

In the next partial step 10b the instructions stored in RIP are changes, and the whole series of events are repeated with the new address and operational mark contained in the new instructions.

3.4 Change of Instructions in RIP. The circuit for changing the instructions in the RIP is represented in Fig.3.4. This comprises the governor of the instruc-

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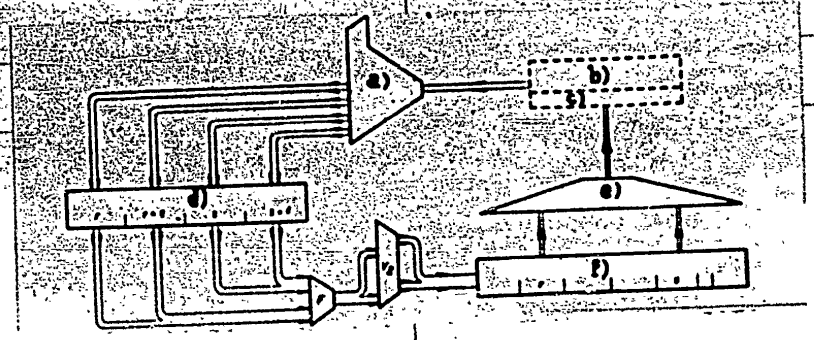

Fig.3.4 - Circuits for Changing Instructions in Governor of Instructional Memory

a) Distributor of output memory; b) Central memory; c) Selective circuit; d) Prepared instructional memory; e) Distributor of addresses; f) Governor of instructional memory

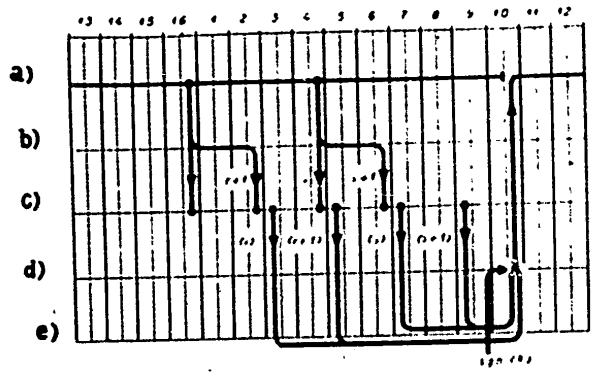

Fig.3.5 - Time Diagram of Action of Circuit from Fig.3.4

a) RIP; b) Distributor of addresses; c) Central memory; d) Router F; e) RIP

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tion memory RIP, the distributor of addresses, the distributor of the output of the memory, the prepared instructional memory PIP, the functional router F and the output router V_2 of the governor of the instructional memory. For completeness the

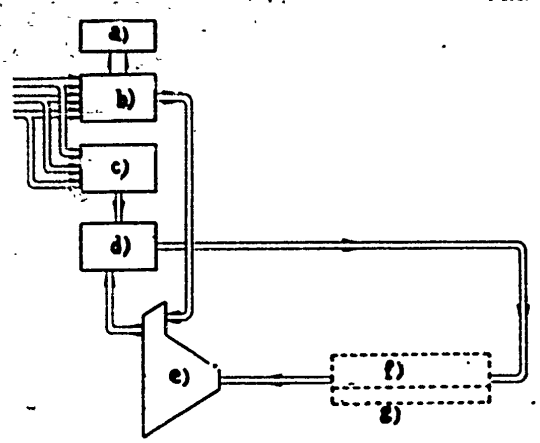

Fig.3.6 - Circuit for Verification of Action of Operation Units and Memories

a) Adder of errors; b) Verifier I; c) Verifier II; d) Verifier; e) Distributor of output of memory; f) Central memory; g) Selective circuit

central memory is also indicated here in dotted lines. The action of the circuit is represented in Fig.3.5.

In partial step 16b the address r goes from the partial memory of the RIP-r via the distributor of addresses to the selective circuit of the central memory. In the next partial step 2b the distributor of addresses assigns this address to the unit and puts the address r + 1 in the memory. Similarly, in partial step 4b the address s and in 6b the address s + 1 are put in the selective circuit of the central memory. According to this address the selective circuit selects in succession

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in the central memory the parts of the next two instructions* and sends them to the distributor of the output of the memory, which is connected in succession with the partial memories of the prepared instructional memory PIP. Thus, into the partial step 3a go the memory PIP-r goes the word <r>, in the partial step 5a to the memory PIP-r + 1 the word <r + 1>, the partial step 7a to the memory PIP-s the word <s + 1> . In the meantime, the operations have proceeded in the operational units and in 9b the results have been verified with respect to their signs in the comparator (see Fig.3.3) as set by the functional router F. The input governor of the instructional memory RIP is connected here via the input router of the RIP with the selected two outputs of the PIP, and in the next potential step 10b this selected instruction goes to the RIP, where it replaces the preceding instruction, whose course has just been described. The new instruction governs the course of the machine in the next working cycle, and remains in the RIP until the end of the next partial step 10a, when it will again be replaced with another instruction.

3.5 Verification of Action of Operational Units and Central Memory. The circuit for verification of the action of the operational units and the memories is represented in Fig.3.6. It comprises: the verification I, the verifier II, the comparator, the adder of errors, and the distributor of the outputs of the memories. For completeness, the central memory is also indicated here in dotted lines. Its action is represented in Fig.3.7. In the partial step 9a the results denoted 1 from all three operational units enter the two verifiers. Verifier II announces the formed correct result, denoted 2, which is sent in the partial step 9b to the comparator. Here it is held until the end of the partial step 13a. Already in the step 9b the same results are sent to the central memory for storage. The announcement of all three results from the operational units, is likewise carried out in

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* As stated in Part 1.3 each instruction is composed of two words stored at two places of the central memory.

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verifier I and ascertained the errors denoted 4, which are signalled in the partial step 9b to the adder of errors, which carries out their evaluation. The announced result, denoted 2, is in the same partial step 9b conducted to the comparator, which is compared with the result 2 from the verifier II. The verification of the correctness of the two verifiers is carried out because the announced results must be in agreement with each other. The recording of the prepared result 2 in the central memory by the normal course of the machine is next carried out. The recording made is immediately read, and the read recording 5 is sent in the partial step 13a to the comparator, where it is compared with the intercepted result 2. The verification of the correctness of the recording in the central magnetic memory is then carried out.

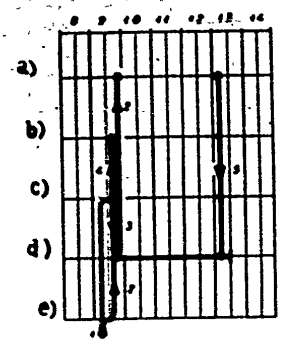

Fig.3.7 - Time Diagram of Action of Circuit from Fig.3.6
a) Central meoory; b) Adder of errors; c) Verifier I; d) Comparator; e) Verifier II

The verifier* is a device which intercepts the results calculated in the three operational units, compares them with each other, "announces" the formed correct result, and ascertains the fortuitous errors in the results from the individual operational units. This occurs separately for each double place. The term "announcement" is defined here as the formation of an output signal in agreement with a majority of the three input signals. The action of verifier I for one double place of interception is presented in the Table of Fig.3.8. The design of the verifier II is similar, but it is also provided with a circuit for ascertain-

* The author of the original circuits of the verifier and the error adder is Vaclav Cerny.

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ment of the errors.

The adder of errors evaluates the errors announced by the verifier I. It has two functions. The first determines whether the results may be regarded as correct, while the second signals to the printer of errors the read errors in the results from the individual operational units. In both cases the adder distinguishes in

a)			b)	c)		
I	II	III		I	II	III
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	1	1	0	1	0
1	1	0	1	0	0	1
1	1	1	1	0	0	0

Fig.3.8 - Action of Verifier for one Double Place

a) Digit from Operational unit; b) Announced digit,

c) Error in operational unit*

each of three results separately: no error, one error, two or more errors. By means of this adder of errors it is assumed that the results announced in the verifier may be regarded as correct:

1) If the results from all three operational units are in agreement;

2) If there is at the most one error in two of the three results at different double places;

3) If there are two or more errors in one of the three results but the other two results are without an error.

The Table of Fig.3.9, which shows when the adder of errors confirms the announced results is constructed on the basis of these conditions. Only the results

* Where 0 means no error, I means an error.

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confirmed by the adder of errors are stored in the central memory. The adder of errors receives the same announcements from the verifier of the operations of the operational units. At the announcement of errors by any of the verifiers of the operations the adder of errors ascertains whether the results from any of the operational units contain two or more errors, and only confirms the result if the results from the remaining operational units are without error. The adder of errors works in the same way when only two of the operational units of the calculator are working and the third one is being corrected.

a)			b)
I	II	III	
0	0	0	ANO
0	0	1	ANO
0	0	2	ANO
0	1	0	ANO
0	1	1	ANO
0	1	2	NE
0	2	0	ANO
0	2	1	NE
0	2	2	NE
1	0	0	ANO
1	0	1	ANO
1	0	2	NE
1	1	0	ANO
1	1	1	NE
1	1	2	NE
1	2	0	NE
1	2	1	NE
1	2	2	NE
2	0	0	ANO
2	0	1	NE
2	0	2	NE
2	1	0	NE
2	1	1	NE
2	1	2	NE
2	2	0	NE
2	2	1	NE
2	2	2	NE

Fig.3.9 - Action of Adder of Errors

a) Read errors in results from operational units*; b) Announced result may be regarded as correct

* Where 0 means no error in result, 1 means one error in result, 2 means two or more errors in result.

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Partial Step	Event	Verification Group	How*	When
10b	Transfer of instructions from PIP to RIP	II	1	11a
	Transfer of f_r to operational units	II	1	11a
10b-11a	Replacement of result (k) in central memory	II	5	13b
11b-12a	Reading of recorded (k) in central memory	II	5	13a
12a	Setting of distributor of addresses	I	4	12b
12b	Transfer of address j to selective circuit of central memory	I	3	13b
	Setting of distributor of outputs of memory	II	4	13a
13a	Transfer of (k) from central memory to comparator	II	5	13b
13b-14a	Reading of (j) in central memory	I	1	15a
14a	Setting of distributor of addresses	I	4	14b
14b	Transfer of address i to selective circuit of central memory	I	3	15b
	Transfer of new address k to address memory P_k	I	6	9b
	Setting of distributor of outputs of memory	I	2.4	15a
15a	Transfer of (j) from central memory to operational units	In operational units		
15b-16a	Reading of (i) in central memory	I	1	1a
16a	Setting of distributor of addresses	I	4	16b
16b	Transfer of address r to selective circuit of central memory	I	3	1b
	Setting of distributor of outputs of memory	I	2.4	1a
1a	Transfer of (i) from central memory to operational units	In operational units		
1b-2a	Reading of (r) in central memory	I	1	3a
2b	Transfer of address r + 1 to selective circuit of central memory	I	3	3b
	Setting of distributor of outputs of memory	I	2.4	3a
3a	Transfer of (r) from central memory to PIP	I	1	9b
3b-4a	Reading of (r + 1) in central memory	I	1	5a
4a	Setting of distributor of addresses	I	4	4b
4b	Transfer of address s to selective circuit of central memory	I	3	5b
	Setting of distributor of outputs of memory	I	2.4	5a
5a	Transfer of (r + 1) from central memory to PIP	I	1	9b
5b-6a	Reading of (s) in central memory	I	1	7a
6b	Transfer of address s + 1 to selective circuit of central memory	I	3	7b
	Setting of distributor of outputs of memory	I	2.4	7a
7a	Transfer of (s) from central memory to PIP	I	1	9b
7b-8a	Reading of (s + 1) in central memory	I	1	9a
8a	Setting of distributor of addresses	I	4	8b
8b	Transfer of address k to selective circuit of central memory	I	3	9b
	Setting of distributor of outputs of memory	I	2.4	9a
9a	Transfer of (s + 1) from central memory to PIP	I	1	9b
	Transfer of results from operational units to both verifiers	I	5	10a
9b	Announcement of errors to adder of errors	I	5	10a
	Transfer of results from verifier I to comparator	I	5	10a
	Transfer of results from verifier II to comparator	I	5	10a
	Transfer of results from cinoaratir to central memory	II	5	13b
	Setting of router F	II	6	10b

* 1 - means verification by unit trial
2 - means verification by agreement between multipath router and distributor
3 - means verification by supplementary agreement in receiver
4 - means verification of path by verification of transmitted signal
5 - means verification with comparator
6 - means verification of agreement of receiver with sender

Fig.3.10 - Survey of Events in Control

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3.6 Survey of Events in Control. The Table of Fig.3.10 presents a survey of the events occurring in the control, which have been described in the preceding paragraphs. Each line of this Table is devoted to one event. The whole represents one working cycle. In the first column of the Table the partial steps are given, in the second brief characterizations of the events, in the third the groups to which the events belong from the viewpoint of the processing of information for errors (see paragraph 3.8), in the fourth the process of their verification (according to paragraph 3.7), and finally in the fifth the partial steps in which the verification occurs. The temporal sequence of the events separately described in the preceding paragraphs can be seen from this Table.

3.7 Verification of Action of Control. A total of six kinds of verification are used in the control of the automatic calculator at different places.

1. Verification by unit trial (parity);
2. Verification by agreement between multipath router and distributor;
3. Verification by supplementary agreement in receiver;
4. Verification of signal path of verification of transmitted signal;
5. Verification with comparator;
6. Verification of agreement of content of receiver with content of sender.

1. Verification by Unit Trial. As explained in detail in the work (Bibl.1), the automatic calculator processes information in the form of words each of which is composed of 32 binary digits. Of the latter 31 are actual carriers of information, while the 32nd digit is formed in such a way that the sum of all 32 digits of the word is an odd number. In this form the words are stored in the central memory of the calculator, and in the same form they are selected and sent to the places where they are needed. The circuit for verifying by unit trial is supplemented with a device which is sensitive to the numerical sum of the received word, and which, if the latter is an odd number, announces its correctness.

By unit trial all of the readings inside the central memory are verified,

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the transfers from the central memory via the distributor of the outputs of the memory to the operational units and to the prepared instructions of the memory PIP, the transfers from the PIP to the governor of the instructional memory RIP, and the transfers from the RIP to the operational units*.

By unit trial the presence of only one error in the event that the error is an odd number can be safely ascertained. This is why it is used when the simultaneous occurrence of several errors is improbable, and when further provisions have been made against the simultaneous occurrence of several errors.

2. Verification by Agreement between Multipath Router and Distributor. The multipath router and the distributor are formed of relays, which must be multiplied at a large number of switching paths because one relay can switch at the most five paths. Due to the failure of some of the relays at the transmission of the words, some of the places are omitted. If these places are units in the transmission of the words the latter are lost. If the number of such lost units is even, the error cannot be found by unit trial. For this reason the multipath and the distribution are supplemented with a circuit which ascertains whether all of multiplied relays are in the same position, that is, whether all of them are on or off, so that they announce in agreement with each other. In this way it is assured that either the whole signal is lost, which is ascertained by unit trial, or that all of the paths are properly connected, so that an error can occur only at failure of one or more individual contacts, which is likewise ascertained by unit trial.

Agreement is verified between router F, the input router V_2 of the governor of the instructional memory and the distributor of the outputs of the memory.

3. Verification by Supplementary Agreement in the Receiver is intended for verification of the transfer of the address from the RIP via the distributor of addresses to the selective circuit of the central memory. At this verification,

* That is, from the reading head to the output memory, see part 2.

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the fact is utilized that each of the addresses is actually sent from the RIP and ~~received in the central memory in two selective circuits (see Part 2), in the one~~ directly and in the other supplementary. The verification occurs by comparing the digits of the address in the two selective circuits for their correspondence with each other. If all of the digits of the same row in both of the selective circuits supplement each other, that is, if in the one circuit there is unity and in the other zero, and conversely, this means that correct transfer has occurred. This verification also catches a plurality of errors. An important fact is that it can also be carried out when the transmitted information is no longer in the transmitter. In this respect it differs from the verification according to 6.

4. Verification of Path by Verification of Transmitted Signal. If a signal traversing any path is verified in the receiver by any verification which catches an error without regard to its number, it is unnecessary to verify separately the proper state of this path. Verification of the path is this case occurs by verification of the received signal. In this way, the path from the RIP to the distributor of addresses, the distributor of addresses*, and the path from the latter to the memory are verified. The path from the memory to the distributor of the outputs of the memory, the distributor of the outputs of the memory*, and the path from the latter of the operational units and the PIP are verified in this way in connection with the verification according to 2.

5. Verification with Comparator. By means of the comparator the circuit for the verification of the action of the operational units and the central memory is verified, as represented in Fig.3.6. With it is also verified the correctness of the recording in the central memory. As can be seen from Fig.3.7 and the description of the action in paragraph 3.5, the results from the operational units are intercepted in two verifiers. From the verifiers it then goes to the com-

* The router is also regarded as the signal path.

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parator (denoted 2 and 3 in Fig.3.7), which carries out the comparison of the two announced results. If these results differ from each other, that is, if there is an error either in one of the verifiers or directly in comparator, and the comparator does not give a signal, then the announced result may be regarded as correct. If everything so far is in order, the announced result 2 intercepted in the comparator is transferred to the central memory, where it is stored, and again verified by reading (in the Table of Fig.3.10 in the partial steps 11b-12a). The read result 5 is again sent to the comparator, where it is compared with the result 2 originally sent from the comparator to the central memory. If these results differ from each other, this means that there is an error either in the path to the memory, in the storage, in the second reading, in the path back to the comparator or finally also in the comparator itself. If the two results are in agreement the comparator gives the signal, and the result may be regarded as correctly stored in the memory.

6. Verification of Agreement between Receiver and Sender. If information given remains stored in the transmitter after it has been transmitted to the receiver, the receiver and transmitter can be supplemented with a circuit for verifying the agreement between their contents. In this way the transmission of the address from the RIP to the address memory P_k is verified (in the Table of Fig.3.10 in the partial step 14b) and the setting of the router F according to the result in the comparator (in the partial step 9b). This verification catches all errors without regard to their number.

3.8 Processing of Information on Errors. This paragraph describes the manner in which the central master reacts to errors, and dissusses the provisions made for eliminating the influence of these errors on the correctness of the whole calculation in the automatic computer. The occurrence of errors announced by the circuits is described in the preceding paragraphs.

All of the events occurring in the control are verified by one of the methods described in paragraph 3.7. The correctness of the course of the events i-

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announced to the central master. If the expected announcement does not occur in a certain moment, this is recorded by the master as an error. The printer of errors records the error, and specifies the place of its occurrence in the machine. If necessary, the kind of operation at which the error occurred is also specified. In this way the correction of permanent defects in the operation of the machine is facilitated. Moreover, the central master is designed in such a way that it is able to eliminate the influence of the ascertained errors on the correctness of calculation proceeding in the automatic computer. The processing of information on errors relating to all of the events of one working cycle is divided into two groups. To the first group belong the events at which there are prepared:

1. In the comparator the verified result of the given operation;
2. In the PIP the new instruction;
3. In the address memory P_k the new address k.

To the second group belong:

1. The storage of the prepared result in the central memory;
2. The transfer of the new instruction from the PIP to the RIP.

This division is used in the "group" column of the Table of Fig.3.10. In general it can be said that the events of the first group are the principal events of the working cycle, while the events of the second group are transitional to the next working cycle. The events of the first group begin in the partial step 12a and end in the partial step 9b of the same working cycle. The events of the second group begin in the partial step 9b of the one cycle and end in the partial step 13a of the next working cycle. By the same division are also divided all of the errors into two groups, and the central master makes a fundamental distinction between errors of the first group and errors of the second group. The master is designed in such a way that at the first occurrence of an error of any group it orders repetition of the whole working cycle, and if the machine again fails to carry out the corresponding events without error, stops the machine. However, the information

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stored in the central memory and the memory of the control remain intact, so that the calculation can be resumed immediately after correction of the defect.

The time diagram of the events at the occurrence of errors of the first group is represented in Fig.3.11. In this diagram are included the events previously represented separately in Figs.3.3, 3.5, and 3.7. In the part denoted A, the normal working cycle governed by the instructions intercepted in the RIP proceeds. In some of the events of the first group of this cycle, errors have been caught. If an error occurs in this group, the central master reacts in such a way as to

1. Prevent storage of the prepared result of the given operation in the central memory;

2. Prevent change of the instruction in the RIP, so that the old instruction remains therein.

These changes are denoted by circles in Fig.3.11. Thus, the circle k_n on the "memory" line at 5 means that the result, which was not confirmed, arrived at the memory but was not stored. The circle at 6 means that the instruction from PIP was prevented from reaching RIP, so that the old instruction was left intact.

The result must not be stored in the memory for the following reasons:

a) If poor information has been used for its formation. This occurs at an error in <i> or in <j>, at an erroneous address, at a poor reading, or at an error in the distributor of the outputs of the memory.

b) The results from the various operational units differ from each other, so that the announced result may not be regarded as correct. This error is announced by the adder of errors (see Table of Fig.3.9).

c) The results, printed in both verifiers, differ (errors in one of the verifiers) so that it is impossible to decide which of the teeth is correct.

d) The address about to be stored is incorrect (error in the address memory P_k or in the address k set in the selective circuit of the central memory), and storage of the result at the wrong place in the central memory would destroy the information

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Fig.3.11 - Time Diagram of Events in Control at Occurrence of Errors in First Group of Events

a) RIP; b) Distributor of Addresses; c) Address memory P_k; d) Central memory; e) Router P; f) PIP; g) Adder of errors; h) Verifier I; i) Comparator; j) Verifier II; k) Operational unit

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previously stored at that place.

~~e) By storage of an incorrect result, the previous content of the corresponding~~ memory would be lost because in that place some of the input values from which the incorrect result was read are stored, so that the calculation could no longer be repeated.

A change of the instruction in the $\bar{R}$IP must be prevented for the following reasons:

a) If a poor information has been used for the preparation of the next instruction in the PIP (at an error in <r>, <r + 1>, <s>, <s + 1>, at an erroneous address, at a poor reading, or at an error in the distributor of the outputs of the memory).

b) If there is an error in the instruction prepared in the PIP (error in the transmission or in the interception).

c) There is no assurance that the recorded result is correct, so that the router F might select an improper instruction.

Therefore, there remains in the $\bar{R}$IP the instruction originally intercepted, so that the machine again carries out the working cycle governed by this instruction. In the event that the error occurring in the preceding working cycle was only fortuitous, the result obtained in this repeated working will be correct, at the same time that the sequence of the instruction prepared in the PIP will remain unchanged. After the repeated working cycle, therefore, the machine proceeds further with the calculation without disturbance.

In the part of Fig.3.11 denoted B, the repetition of the whole working cycle (at which the repeated events are indicated by dotted lines) is represented. If up to this time everything has occurred without error, the master permits storage of the new result in the memory, and replacement of the instruction in the $\bar{R}$IP with the instruction from the PIP. The next working cycle according to this new instruction is denoted C in Fig.3.11. If an error also occurs at this repeated cycle B, the master stops the whole computer, and announces this action to the signal board.

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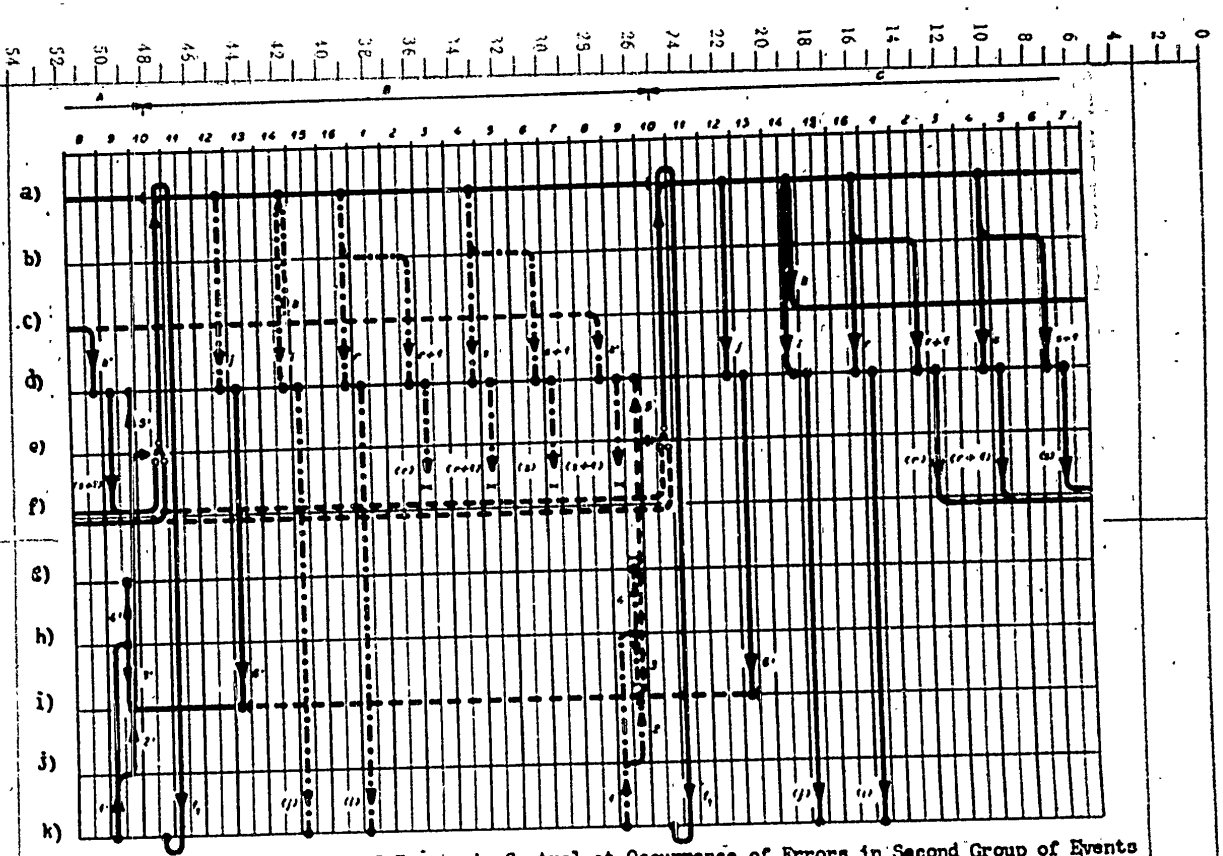

Fig.3.12 - Time Diagram of Events in Control at Occurrence of Errors in Second Group of Events

a) $\overline{R}$IP; b) Distributor of addresses; c) Address memory P_k; d) Central memory; e) Router F; f) PIP; g) Adder of errors; h) Verifier I; i) Comparator; j) VerifierII; k) Operational unit

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Excepted from the described process are the events relating only to the ascertainment of the errors in the verifiers. Since a circuit for verifying the correctness of the whole calculation is concerned here, it is unnecessary to repeat the working cycle at the occurrence of errors (that is, the cycle B in Fig.3.11), because the machine stops immediately and announces the disturbance.

After the machine has stopped because of an error, the last instruction carried out remains intercepted in the $\bar{R}IP$. This enables resumption of the calculation after correction of the defect in the machine. Since the ascertained error did not lead to any disturbance of the information stored in the central memory, the calculation after the correction is continued simply by carrying out the instruction which has remained intercepted in the $\bar{R}IP$.

The time diagram of the events at the occurrence of errors in the second group is represented in Fig.3.12. At the end of the working cycle denoted A in the figure, errors have occurred in some of the events of the second group. To these errors the central master reacts as follows:

1. Retains in the comparator the correct result (denoted 2' in Fig.3.12) obtained in the preceding working cycle A.

2. Retains in the address memory P_k the old address (denoted k') stored in that place in the preceding working cycle A.

3. Retains in the prepared instructional memory PIP the instruction stored in that place in the preceding working cycle A.

The result 2" from the working cycle A is retained in the comparator because it is not certain whether it can be correctly stored in the central memory, and its incorrect storage might destroy in the memory the information from which it was obtained. The address k' is retained in order to be able to retain the result newly stored in the central memory. The instruction is retained in the PIP because it is not certain whether the selected instruction was correctly transmitted to the $\bar{R}IP$, so that in case of an error there would be no intercepted instruction with which

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to continue the machine.

In the next working cycle B the master prevents storage of the new information in the comparator, in the address memory P_k, and in the PIP. At its conclusion the machine again transmits the address k' to the central memory, stores in the latter the result 2' intercepted from the preceding cycle A in the comparator, and transmits the selected instruction from the PIP to the $\bar{R}$IP. The events of this cycle, B which are indicated by dotted lines in Fig.3.12, proceed normally according to the instruction present in the $\bar{R}$IP at the time. Since there is no assurance of the correctness of this instruction, the transmission of the address k to the address memory P_k, the transmission of <r>, <r + 1>, <s>, <s + 1> from the central memory to the PIP, the transmission of the result of the operation from the verifier to the comparator, and the evaluation if the error in the adder of errors are prevented. In the figure these interventions are denoted by circles. The events of the first group in this cycle B are not verified (with the exception of the resetting of the address k' in the selective circuit of the central memory) because the correctness does not depend on them.

At the close of working cycle B, the intercepted results 5' are again stored in the central memory and the selected instruction is transmitted from the PIP to the $\bar{R}$IP. If the events of the second group proceed this time without error, then the course of the next working cycle is again normal. If the central master catches an error in more than one of the events of the second group, the machine stops, and announces the fact to the signal board. In this case, the last correct result remains intercepted in the comparator, in the address memory P_k the address k' of the memory in which it has been impossible to store the result, and in the PIP the last correct instruction, according to which it has been impossible to continue. This information, after correcting the defect, enables the calculation to proceed further without any loss of time or for as long as the operation of the automatic computer is continued.

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Input of Information to Machine

Before beginning the calculation, the starting information must be stored in the central memory of the automatic calculator, composed of the instructional network and the starting numerical values of the problem. The first instruction must also be stored in the governor of the instructional memory according to which the machine will be governed in the first working cycle after starting. The storage of this information in both the central memory and the governor of the instructional

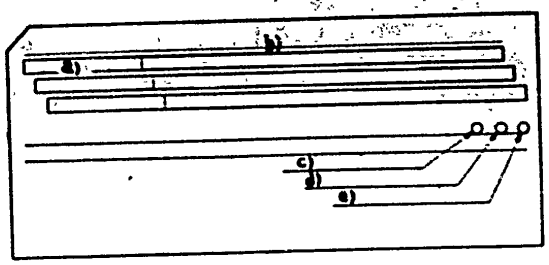

Fig.3.13 - Arrangement of Information on Perforated Cards of Input Unit of SAPO

a) Address; b) Word; c) Store in $\bar{R}$IP/I; d) Store in RIP/II; e) Read next card

memory is carried out by the input unit connected with circuit of the control, as represented in Fig.3.14 and 3.16.

3.9 Perforated Cards. All of the necessary information is preperforated on perforating cards. In one perforated card the following are perforated:

1. The word to be stored in the machine;
2. The indication of the place where the word is to be stored. This may be:
   - 2.1 The address of the place in the central memory;
   - 2.2 The command to store the word in the first half of the $\bar{R}$IP;
   - 2.3 The command to store the word in the second half of the $\bar{R}$IP.

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3. The command: "read to the next card!"

The word to be stored in the machine is perforated on the card three times. This enables verification not only of the errors occurring at the perforating but also of the mechanism and the circuit of the input unit. The address of the memory at which the word is to be stored is also perforated three times on the card, and is further supplemented by the signal of the unit trial (parity). The commands 2.2,

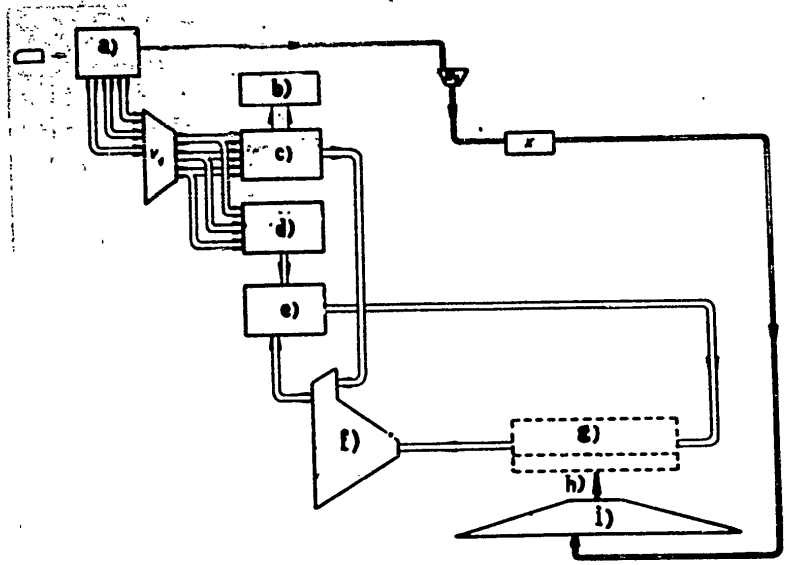

Fig.3.14 - Circuit for Storage of Information from Cards in Central Memory

a) Input unit; b) Adder of errors; c) Verifier I; d) Verifier II; e) Comparator; f) Distributor of outputs of memory; g) Central memory; h) Selective circuit; i) Distributor of addresses

2.3, and 3 are perforated in the form of similar holes only one time each. In the card carrying the command to store the word in the given half of the RIP, of course, the address is not perforated. The arrangement of all of the information on the

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card can be seen from Fig.3.13. This figure shows that the given information occupies only the upper half of the card. In the lower half, other data in the normal Powers code can evidently also be perforated, and the cards can also be processed with the current Aritma or Powers machine.

3.10 Input Unit. The input unit is started either manually or automatically during the calculation according to the corresponding instruction in the instructional network (code G, see [1]). By starting manually the mechanism of the input unit is fed card after card as they come in the magazine, and the given information is stored in the corresponding memory. This continues until the magazine is emptied of prepared cards, and then stops automatically. By starting automatically with the code G, the calculation is interrupted in the calculator, the mechanism of the input unit is fed one card, and the given information is stored in the given memory. If the command "read the next card!" is also perforated on this card, the next card is fed and is treated in the same way. Thus, all of the cards perforated with this command are read in succession. Then the input unit stops, and the further calculation starts automatically in the automatic calculator.

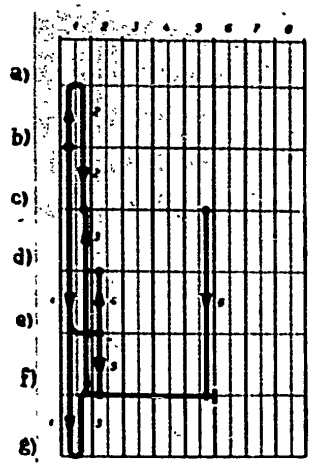

Fig.3.15 - Time Diagram of One Working Cycle at Storage of Information from Cards in Central Memory

a) Address memory X; b) Input unit; c) Central memory; d) Adder of errors; e) Verifier I; f) Comparator; g) Verifier II

The action of the input unit proceeds in a working cycle composed of eight steps, each divided into two partial steps a and b. These 16 partial steps form one working cycle of the input unit. During one working cycle, the information

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from one perforated card is taken and stored. Then the mechanism of the input unit stores the read card and prepares the next card. The working cycle of the input unit differs from the working cycle of the control in both length and composition.

3.11 Input to Central Memory. The circuit for the storage of information from the cards in the central memory of the automatic calculator is represented in Fig.3.14. Here are: the input unit, the input router of the distributor V_1, the two verifiers, the adder of errors, the comparator, the distributor of the outputs of the memory, the address router W_1, the address memory X, and the distributor of addresses. For completeness the central memory is also indicated in the figure. Before beginning the working cycle of the input unit, the input router of the verifiers is switched to the position in which the input unit is connected with the inputs of both verifiers. The input unit is also connected via the address router W_1 with the address memory X. The time diagram of one working cycle is represented in Fig.3.15. In the partial step 1a the perforated word is taken on the one hand and on the other hand the address from the card. The word 1 goes from the input unit to the two verifiers, the address 2 to the address memory X. The address 2 is in the partial step 1b sent from the address memory X to the selective circuit of the central memory*. In the partial step 1b the announced word 3 goes to the comparator and from there immediately also to the central memory, where it is afterward stored at the given address. In the partial step 2a the verifier I announces the error 4 to the adder of errors and at the same time sends the announced word 5 to the comparator, where this word 5 is compared with the word 3 from verifier II. Then, if everything is in order, the word is stored in the central memory. Immediately afterward the stored word 6 is again read and sent to the comparator.

3.12 Input to Governor of Instructional Memory. The storage of the information from the cards in the governor of the instructional memory RIP is carried by the

* The selective circuit is for operating the input unit via the address distributor permanently connected with the address memory X.

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circuit represented in Fig.3.16. Here are: the input unit, the input router of the verifiers V_1, the two verifiers, the adder of errors, the comparator, the distributor of the outputs of the memory, the input router V_2 of the governor of the instruc-

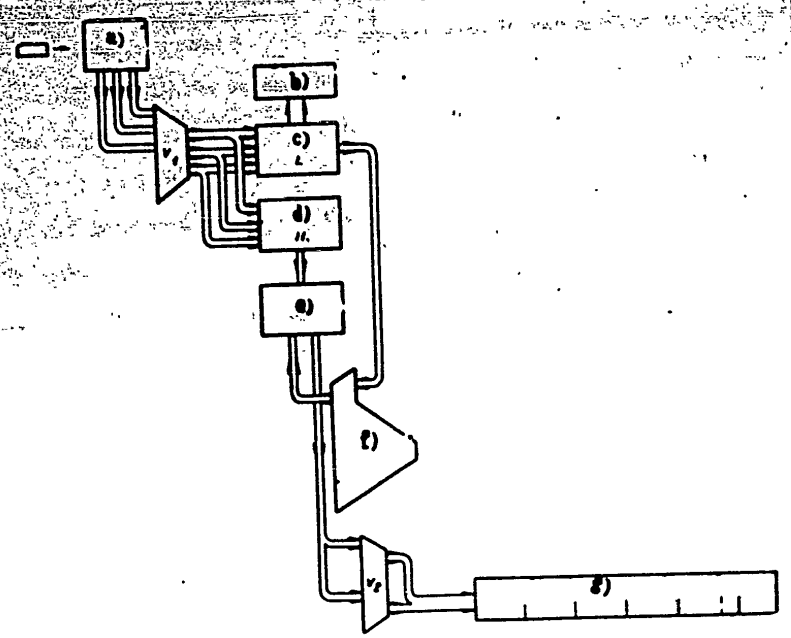

Fig.3.16 - Circuit for Storage of Information from Cards in Governor of Instructional memory

a) Input unit; b) Adder of errors; c) Verifier I; d) Verifier II; e) Comparator; f) Distributor of outputs of memory; g) Governor of instructional memory

tional memory and the governor of the instructional memory. By this operation the router V_1 connected the input unit permanently with the inputs of the two verifiers, and the distributor of the outputs of the memory connects the verifier I with the comparator. The time diagram of one working cycle is represented in Fig.3.17.

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In the partial step 1a the perforated word 1 is read and sent from the input unit to the two verifiers. In the same partial step is also perforated the command 2 specifying in which half of the $\overline{RIP}$ the read word is to be stored. According to this command the router V_2 connects the corresponding part of the $\overline{RIP}$ with the given output of the comparator. In the partial step 1b the announced word 3 goes from the verifier II to the comparator. In the partial step the announced word 4 goes to the comparator from the verifier I and at the same time the announced error 5 goes to the adder of errors. In the next partial step 2b the word 6 from the comparator is stored at the corresponding place in the $\overline{RIP}$ and this completes the whole operation.

3.13 Verification of Input Unit. Similarly as in the working cycle of the control, all of the events of the working cycle of the input unit are verified. A survey of the events and their verification is presented in the Table of Fig.3.18. The verification is of the type described in paragraph 3.7. Here the processing of the information on the ascertained error is very simple; when an error occurs, the input unit stops automatically and announces the error.

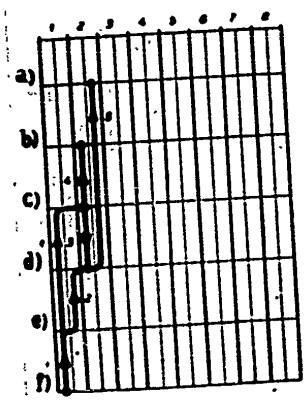

Fig.3.17 - Time Diagram of One Working Cycle at Storage of Information from Cards in Governor of Instructional Memory

a) $\overline{RIP}$; b) Adder of errors; c) Verifier I; d) Comparator, e) Verifier II; f) Input unit

Output of Information from Machine

The output unit perforates the results calculated by the machine in perforating cards. The information coming either from the central memory or directly from the operational units is perforated in the cards.

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3.14 Perforated Cards. The arrangement of the information on the employed perforated cards must be such that the cards can afterward be used for the storage of this information by the input in the central memory of the calculator. On the

a)	b)	c) d)	c) e)
1a	f)	5	2b
	g)	1	2b
1b	h)	3	2b
	i)	5	2b
2a	j)	5	2b
	k)	5	3b
2b	l)	1	control
3a—3b	m)	5	6a
4a—4b	n)	5	6a
5a	o)	5	6a
5b	p)	5	6a

Fig.3.18 - Survey of Events at Action of Input Unit

a) Partial step; b) Event; c) Verification; d) How*; e) When ; f) Transmission of word from input unit to both verifiers; g) Transmission of address from input unit to address memory X; h) Transmission of address to selective circuit of central memory; i) Transmission of announced word from verifier II to comparator; j) Transmission of announced word from verifier I to comparator; k) Announcement of error to adder of errors; l) (Transmission of part of instruction from comparator to $\bar{R}IP$); m) Recording of word in central memory; n) Verifying reading of recorded word; o) Setting of distributor of outputs of memory; p) Transmission of word from central memory to comparator

perforated cards are outlined fields for the following information:

1. The word perforated in the card by the output unit.

2. The address of the memory from which this word was taken.

* 1 - verification by unit trial, 3 - verification of supplementary agreement in receiver, and 5 - verification with comparator

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3. The index by which the output unit denotes the sequence of the card.

4. The command: "perforate the next card!"

The arrangement of this information on the punched card can be seen from Fig.3.19.

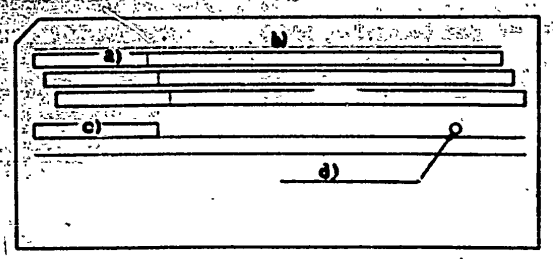

Fig.3.19 - Arrangement of Information on Perforated Card for the Output Unit of the SAPO

a) Address; b) Word; c) Index; d) Perforate next card

3.15 Output Unit. The output unit together with the corresponding circuit carries out the following operations:

1. Output from central memory according to addressed preperforated in the card.

2. Output from operational units.

From the central memory output, the mechanism of the output unit receives the prepared card from the magazine, reads the address perforated in the card, according to this address finds the place in the central memory of the calculator and stores at that place the word perforated in the same card. Then the perforated card is discharged. For carrying out these operations the output unit may be either manual or automatic. When starting manually, the output unit carries out these operations as long as there are cards in the magazine; when there are no more cards it stops automatically. When starting automatically, these operations are carried out according to the instructions of the code H (see [1]). During this starting the

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calculation in the calculator is interrupted, and the output unit carries out the described operations until it encounters a card provided with the command "perforate next card!" Then the output unit stops automatically, and calculation in the calculator is resumed.

At the output from the operational unit, the output unit perforates in the prepared perforated card the word which has just come out of the operational unit. After being perforated the card is automatically discharged, and the next one is taken. This operation is carried out only automatically according to the instructions of the code H. The whole operation proceeds in parallel with the operations governed by the control, whose action continues without further interruption. In this respect, the operations of the output unit differ from the operations described in the preceding paragraphs and from the operations carried out by the input unit.

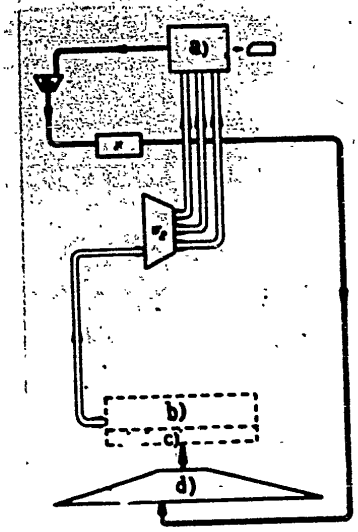

Fig.3.20 - Circuit for Storage of Information from Central Memory in Perforated Cards

a) Output unit; b) Central memory; c) Selective circuit; d) Distributor of addresses

All the cards passing through the output unit are provided by this unit with an index. The index is a 12-place number in the binary system, which is increased by unity after each automatic starting of the output unit. In this way it is assured that the card in which there is finally stored the whole result of the calculation of the automatic calculator, is clearly identified with respect to the sequence of its passage through the output unit.

The action of the output unit proceeds in a working cycle similar to that of

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the input unit.

3.16 Output from Central Memory. The taking of information from the central memory to the perforated card is carried out by the circuit represented in Fig.3.20. Here are: the output unit, the address router W_1, the address memory X, the distributor of addresses, and the router of the output unit W_2. For completeness the central memory is also indicated in dotted lines. Upon the execution of the operations, the two routers and the distributor of addresses are in such positions that they are connected with each other in the manner shown in Fig.3.20. Here the router W_2 of the output unit connects all three of its outputs in parallel.

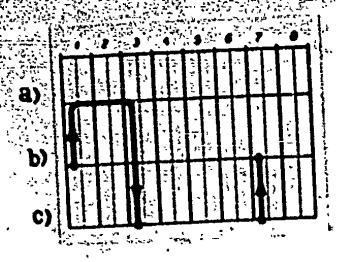

Fig.3.21 - Time Diagram of One Working Cycle at Storage of Information from Central Memory in Perforated Card

a) Address memory X; b) Output unit; c) Central memory

The time diagram of one working cycle at the storage of information from the memory in the perforated card is represented in Fig.3.21. In partial step 3a, the address is read from the perforated card and intercepted in the address memory X. In the partial step 3a this address is transmitted to the selective circuit of the central memory. Then the perforated card in which this address is perforated moves on the perforator and in the partial step 7a the corresponding word goes from the central memory to the perforator of the output unit and is perforated in the prepared card. Then the perforated card is filed in the filing magazine, and the mechanism feeds the next card to the reading device.

Upon the execution of the described operations, the read address is verified by unity trial and transmitted to the address memory X. The setting of the address in the selective circuit of the central memory is verified by supplementary verification of the agreement in the receiver. The reading in the central memory is ver-

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ified by unity trial. The proper action of the perforator is ascertained by triple perforations and verified by unity trial. Here also at the automatic starting of the output unit the prepared perforated cards in the magazine are verified. Upon finding any defect the master stops further action of the output unit, and, if necessary, prevents further starting of the calculation in the computer, and announces the found defect.

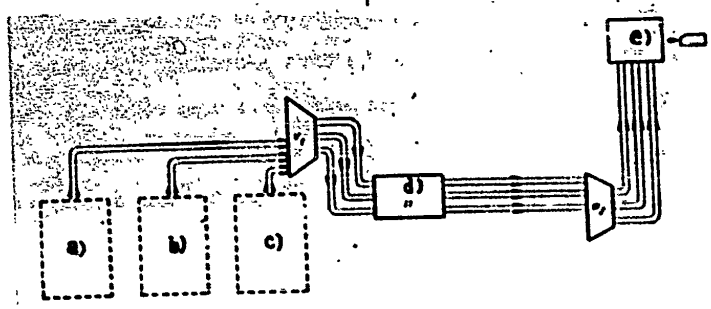

Fig.3.22 - Circuit for Storage of Information from Operational Units in Perforated Cards

a) Operational unit I; b) Operational unit II; c) Operational unit III; d) Verifier II; e) Output unit

3.17 Output from Operational Units. The storage of information from the operational units in the perforated cards is carried out by the circuit represented in Fig.3.22, in which, for completeness, the operational units are also indicated by dotted lines. In this operation the operational units, the output router of the verifiers V_1, the verifier II, the router of the output unit V_2, and the output unit participate. Here the two routers are in positions at which they connect the paths, as represented in Fig.3.22. All of the events of these operations are governed directly by the control and proceed simultaneously with the normal action of the latter, in such a way that the result of the operations from the operational units,

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intercepted in the verifier II, are sent unchanged in the partial step 11a via the router W_2 to the output unit. Simultaneously, the normal storage of the announced result in the central memory proceeds according to the instruction in the RIP, as described in paragraph 3.3. Then the output unit perforates the result, files the card, and is fed with the next clean card.

At the execution of these operations, all of the previously described verifications of the control are in action. It is further ascertained whether a prepared card is in the output unit to be perforated, and whether the output unit is in the starting position. The latter verification is necessary because the mechanism of the output unit works more slowly than the working cycle of the control, so that the control might order the next perforating before the end of the preceding perforating. If for any reason the next card is not ready, or if the command to perforate arrives ahead of time, the whole computer is stopped. The last executed instruction remains intercepted in the RIP and in the verifier the last result, which could not be perforated.

4. Operational Units

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Received: November 23, 1953

Introduction

4.1 Introduction. The operational unit is the part of the automatic computer which, according to the command from the control, carries out with the given work the prescribed operation.

Detailed descriptions of the codification of words (numbers, instructions, logical numerical symbols) in the Czechoslovakian automatic computer, together with lists of the principal operations carried out, will be found in the literature (1.2).

In this part we shall describe in detail the individual operations from the

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mathematical viewpoint and outline the functioning of the universal operational unit at the individual operations.

During formulation of the mathematical principles, the fact was borne in mind that of the four fundamental mathematical operations, the most difficult for the automatic computer is division. The method of operation was formulated in such a way that the whole device for carrying out division could also, with minor modifications, be used for all of the remaining operations. The selection of movable place commas greatly diminished the difference in the difficulty of the individual operations.

Of course, for the separate execution of any of the described operations, without regard to the remaining operations, it would have been possible to find a simpler method than the one adopted. This, however, would have required the use of a special operational unit for each of the operations. The cost of building such special operational units, however, would be much higher than the cost of building one universal operational unit, which carries out all of the operations, although by a more complicated method.

Group Scheme of Operational Units

4.2 Group Scheme of Operational Units. The operational unit of the Czechoslovakian automatic computer is represented in a simplified group scheme in Fig.4.1. The most important circuits of the operational unit are according to their logical and functional interdependence combined into groups, indicated by rectangles with the inscribed denotation of the group. The individual groups are connected with each other by signal conductors. The signal conductors, indicated in the scheme by solid lines, mediate the transmission of the information: the wider double lines denote multipath signal conductors; the narrower double lines denote paths of exponents, corrections, etc; and by the simple lines the paths of the signs are indicated. ~~The signal paths indicated by dotted lines are the mastering and signalling paths.~~

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Next we briefly describe the functions of the individual parts of the operational unit.

The Memory of Operational Marks governs directly the action of the operational unit. This memory receives from the control, before each operation, the corresponding operational mark f_1. According to this mark, the selection of the electrical pulse necessary for the execution of the given operation, and its connection at the corresponding place of operational unit, is carried out.

The Central Generator of Pulses gives the electrical pulses, of which there are nearly a hundred kinds. The individual pulses are composed of impulses. The pulses differ from each other in the length of their impulses and in their position in the working cycle of the machine.

Input Memories VPi, VPj. In these memories of the operational unit, the words <i> and <j> on which the operation is to be carried out, are received from the control. From the two memories VPi and VPj signal paths lead to the remaining parts of the operational unit. The selection of these paths is governed by the memory of operational marks according to the kind of operation to be carried out.

The Input Circular Displacer dominates the memory of operational marks. Through the displacer the word entering the memory VPj passes. If the circular displacer is at rest, the word enters the memory VPj unchanged. If the displacer is in action each binary digit of the word <j> enters the memory displaced by n places to the left, at which n ordinal higher digits enter at n lower places of the memory VPj. The magnitude of displacement n is governed by the kind of operation.

The Comparator of Multiples is a very important part of the operational unit, and participates in nearly all of the operations. It is composed of 15 29-place adders with memories. In the figure the individual adders with memories are denoted by the numbers 1 to 15. Its name is derived from one of the most complicated events proceeding in the comparator at division. This is the formation of simple multiples, double multiples, etc. up to 15-fold multiples from 1-16 numbers which enter the

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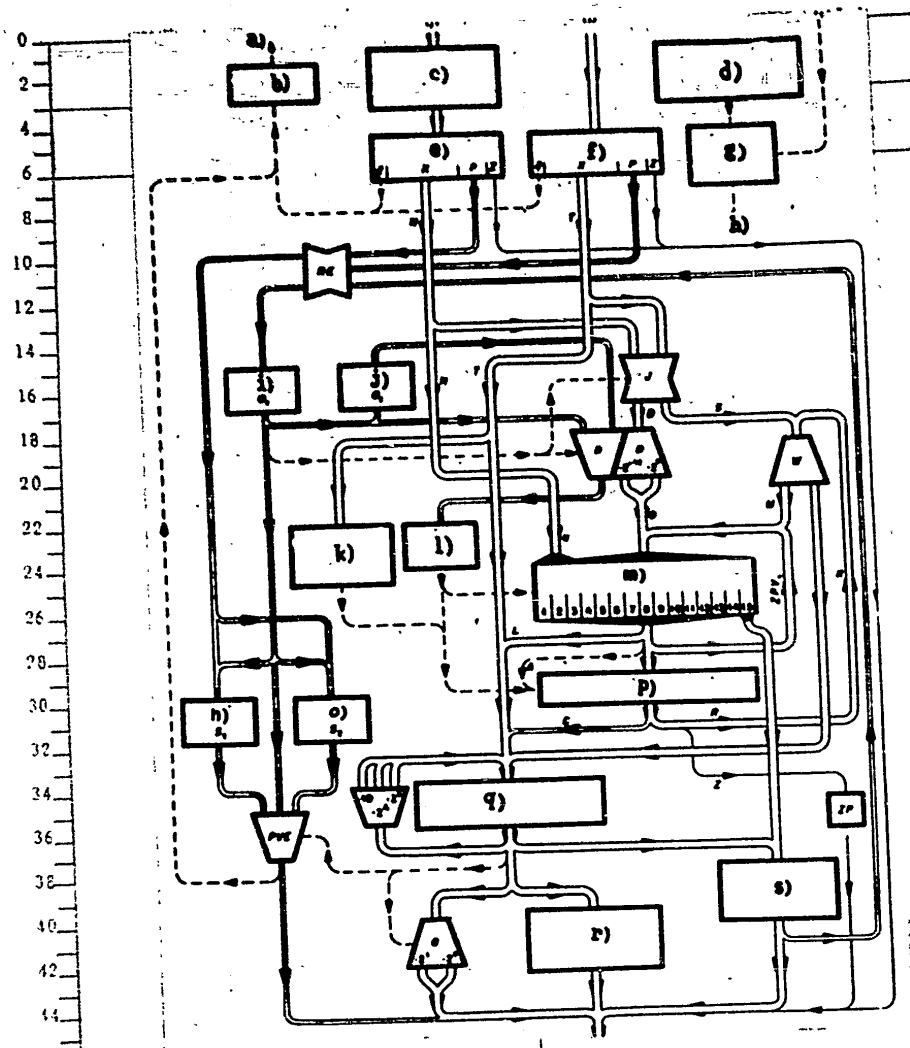

Fig.4.1 - Group Scheme of Operational Unit

a) Correctness of operation; b) Verifier of operations; c) Input circular displacement; d) Central generator of impulses; e) Input memory VPj; f) Input memory VPi; g) Memory of operational mark; h) Selective pulse; i) Subtractor O_1; j) Subtractor O_2; k) Transformer of multipliers; l) Selective decorder; m) Comparator of multiples; n) Adder S_1; o) Adder S_2; p) Searcher of boundaries; q) Result saver; r) Output circular displacer; s) Displacer of result

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comparator by the conductor N and the comparison of these multiples with the half values of the numbers which enter the comparator by the conductor M. The comparison is carried out by subtraction in the individual adders. Concerning the sign of the difference in the individual adder, the comparator gives the signal via the conductor to the searcher of boundaries. The output of the comparator of multiples is, moreover, connected with the input of the comparator via the conductor of the return connection ZPV_1.

The searcher of boundaries dominates the output signal path (conductor R) from the comparator of multiples in such a way that the transmission of only the smallest positive difference of all the differences formed by the comparator is possible.

The Result Saver forms a plurality of operations, the final result by summing the individual partial results obtained during the operations. It is provided with a return connection via the conductor ZPV_2. The binary number passing through this conductor is automatically multiplied by a given constant, whose value is governed by the kind of operation (10, 2^4 or 2^5).

The displacer of the results carried out at a plurality of operations the displacement of the result in such a way that the first unity of the result stands immediately after the place comma. The magnitude of the displacement is signaled to the subtractor O_1.

The Transformers of Multipliers at the operation of multiplication changes the signal depicting the multiplier into the signal which dominates the searcher of boundaries.

The Subtractor O_1 carries out the comparison of the magnitudes of the exponents of the numbers entering into the operations. According to the sign of the result the router dominates in another signal path. It forms the output values for the adders S_1, S_2 and for the selective decoder.

The selective decoder at a plurality of operations is dominated by the searcher of boundaries.

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The Subtractor O_2 receives as input values positive binary numbers from the subtractor O_1. Certain constants of the value 12 of the mentioned input values are stored. The result is transmitted to the selective decoder.

The verifier of operations verifies the correctness of the course of each individual operation*. After the end of the operation, the control transmits the resultant information as to correctness.

The output circular displacer is connected with the output conductor which brings the result of the operation from the operational unit to the control. Its functioning is attuned with the input circular displacer. It always carries out the same circular displacement as the input displacer but in the opposite direction.

Further details will be given at the description of the individual operations.

Operations of Automatic Computer

4.3 Survey of Codes. The operations of the automatic computer are fully defined by the working process by which the machine during one working cycle forms the resultant information from the given information.

The machine receives the information in the form of words. By words there may be expressed either numbers or half instructions or logical numerical symbols.

The numbers may be depicted by two different codes: Code B or Code D.

According to Code B the number N is expressed by three binary numbers X, P, Z, at which there is valid

$$N = (-1)^{Z} \cdot X \cdot 2^{P},$$

where the 24-place binary numerical picture X is in the range of $2^{-1} \leq X < 2^{0}$ (the first unity of the picture is immediately after the place comma); the exponent P is expressed in the binary system of 5-place positive numbers with their sign and

* The correctness of the operation does not yet guarantee the correctness of the

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in the range of $-31 \leq P \leq 31$; the sign $Z = 0.1$.

According to Code D the number N is expressed by the three numbers Y, Q, Z, for which the following is valid:

$$N = (-1)^{z} \cdot Y \cdot 10^{Q},$$

where the 24-place binary numerical picture Y is composed of six decimal digits expressed by six-four-place binary numbers and in the range of $10^{-1} \leq Y < 10^{0}$; the exponent Q is expressed in a binary system of five-place positive numbers with sign and in the range of $-9 \leq Q \leq 10$; the sign $Z = 0.1$.

The instruction contains the instruction for the operations and five addresses. These six informations are expressed by six binary numbers, which are divided into two words. Each of the two words, which together form the instruction, contains three binary numbers, which are generally denoted by the letters A, B, and C. The number A is 10-place, the number B 9-place, and the number C 12-place.

The logical numerical symbol is expressed by a 23-place binary number. At the remaining eight places of the word there are always zeros (blind places).

Each word (number, half instruction or logical numerical symbol) is provided with a special binary digit, called parity, which enables verification of the correctness of the word transmitted to the machine. The mark ? denotes in the word the place reserved for parity.

For further information on the codes of the numbers and instructions the reader is referred to the work (1). On the codes of the logical numerical symbols, see word (2).

The automatic computer carries out three kinds of operations:

a) Arithmetical operations (that is, positive mathematical operations with numbers and transformation).

Operational marks:

S Addition with correction

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ST	Addition without correction
SM	Subtraction with correction
SMT	Subtraction without correction
N	Multiplication with correction
NT	Multiplication without correction
D	Division with correction
DT	Division without correction
T	Transformation

b) Nonarithmetical Operations (that is, other working procedures at which there are reformed or formed instructions or numbers).

Operational marks:

SX	Detachment of exponent
WX	Replacement of the exponent
SYZ	Detachment of the sign
WYZ	Replacement of the sign
SXY	Detachment of the number A
SZ	Detachment of the number B
SY	Detachment of the number C
SWYZ	Attachment of the number A in the instruction
SWZ	Attachment to the number B in the instruction
SWY	Attachment to the number C in the instruction
WXY	Replacement of the number A in the instruction
WZ	Replacement of the number B in the instruction
WY	Replacement of the number C in the instruction

c) Logical Operations (that is, operations with logical numerical symbols).

Operational marks:

DS	Combination
WD	Penetration

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KDS Supplementation

The description of each of the arithmetical operations is divided into two parts. In the first part the mathematical principles of the operations are described that is, with the help of which partial operations with the numbers the machine carries out the given operations. The course of the events in the operational unit is discussed in the second part of the description. For greater clarity, examples are also included.

With the nonarithmetical and logical operations, the principles and the events in the combined operational units are described.

In the further text, in order to distinguish unity in the decimal system from unity in the binary system, the mark I will be used for unity in the binary system.

Arithmetical Operations

4.4 Compounding.

Operational marks:

S	Addition with correction
ST	Addition without correction
SMT	Subtraction without correction
SM	Subtraction with correction

Mathematical Principle of Compounding. Compounding is addition or subtraction of two numbers with respect to their signs. The difference between addition and subtraction is insignificant. The differences are mentioned at the corresponding places in the text.

The numbers <i> and <j> to be added are expressed according to code B by two triple numbers X_i, P_i, Z_i, and X_j, P_j, Z_j, as explained in paragraph 4.3. The machine forms the number <k> in such a way that <k> = <i> + <j> (or at subtraction <k> = <j> - <i>). The number <k> is likewise expressed according to code B by the triple number X_k, P_k, Z_k.

We describe first the formation of the binary numerical picture of the sum X_k

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of the sign Z_k and then the formation of the resultant exponent P_k.

First we divide the binary numerical pictures X_i, X_j of the numbers <i>, <j> by two (that is, we displace both of the numerical pictures with respect to the place comma by one place to the right (see the examples of Figs.4.2 and 4.3). Since X_i, $X_j < 1$, therefore $X_i/2$, $X_j/2 < 0.5$; this assures that the sum of these corrected numerical pictures will always be less than one. Therefore, the binary numerical picture of the addition is left unchanged. The numerical picture of the second af the two additions is further moved displaced to the right by as many places as its exponent P is smaller. By this means the places of the two numerical pictures belonging to the same order of both numbers (but not the same order of both pictures!) lie below each other. We calculate the sum of these two displaced numerical pictures at 29 binary places (for simplicity the example is carried out at only 26 binary places). (At subtraction we affix the binary supplement of the numerical picture X_i, as shown in the appendix.) The sum is formed in the absolute value, where we get the number X'_k. At the same time we form the signed digit Z_k.

The sum X'_k is arranged in such a way that only the first 24 binary digits after the place comma are retained, that is, whether without or with correction. The correction is carried out in two steps with regard to the position of the first unity of the sum X'_k with respect to the place comma, as follows:

In the first step we assign unity to the 26th place after the order comma of the sum X'_k. If, after this step, the result does not have unity at the first place after the order comma, we do not carry out the second arranging step but retain further only the 25 highest places of the sum X'_k.

If, after the first arranging step has been carried out, the result has unity at the first place after the order comma, we carry out the second arranging step by again assigning unity to the 26th place (thus we assign in both steps in all + 1 to the 25th place). In this case, we retain further only the 24 highest places of the arranged sum X'_k.

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The operation is completed in such a way that we displace the sum X_k so that its first unity stands immediately after the order comma, where we get the numerical picture X_k of the result.

We calculate the exponent P_k with respect to all of the executed order displacements. Here we start with the greater of the two exponents P_i, P_j. From it we subtract the correction $\Delta - 1$, where Δ is a positive number giving the number of places by which X_k must be displaced in order to obtain X_k and unity or we divide both pictures X_i, X_j by two at the beginning of the operation. If the sign of the difference $P_i - P_j$ is positive, the value of the corrected exponent gives the resultant exponent P_k. If the sign of the difference $P_i - P_j$ is negative, we obtain P_k after changing the sign of the corrected exponent with the opposite sign.

<u>Method of Compounding in Operational Unit</u>. The two numbers <i> and <j>, given by the triple numbers X_i, P_i, Z_i and X_j, P_j, Z_j, enter the input memories of the operational unit VPi and VPj. The verifier of operations investigates by so-called unity trial whether both words have been received without error. Here it is ascertained whether the number of unities in both of the two words is odd.

From the memories VPi and VPj the exponents P_i and P_j go via the distributor of exponents RE to the subtractor O_1, which calculates the difference $P_i - P_j$. The information on the sign of the difference is intercepted in the memory of the subtractor until the end of the whole operation. The value of $P_i - P_j$ is on the one hand retained by the subtractor O_1 in its memory and on the other hand sent (in absolute value) to the subtractor O_2. The subtractor O_2 calculates the difference $|P_i - P_j| - 12$, which remains in its memory. If the sign of the difference $P_i - P_j$ is positive, J remains in the resting position; in this case the output conductor T from the memory VPi is connected with the conductor S and the output conductor N from the memory VPj with the conductor D. At a negative sign of the difference $P_i - P_j$ the crossing switch J is switched. The conductor T is then connected with the conductor D and the conductor N with the conductor S.

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If in absolute value the difference $|P_i - P_j| < 12$, the order displacer D connected with the conductor D comes into action. The number which then passes through the order displacer D is divided by the constant 2^{12} (is displaced by 12 places to the right). If in absolute value the difference $|P_i - P_j| < 12$, the displacer D remains at rest, and the number passes through it unchanged.

If the order displacer D is in action, its second part switches the input of the selective decoder from the output of the subtractor O_1 (in whose memory there is the value $P_i - P_j$) to the output of the subtractor O_2 (which has in its memory the value $|P_i - P_j| - 12$). The function of the selective decoder will be described later.

The half values of the numerical pictures X_i, X_j (for example, their binary supplements, which depend on the signs of Z_i and Z_j and on whether addition or subtraction is concerned) depart from the memories VPi and VPj via the crossing switch J. The half value of the picture to which belongs the greater exponent P, passes through the crossing switch J to the conductor S, the router W and the conductor H to the left input of the adders 3 to 15 of the comparator of multiples. The half value of the second picture passes through to the conductor D and via the order displacer D to the right input of the adders 4 to 15 of the comparator of multiples. The conductor D is connected with the comparator of multiples in such a way that the numerical picture enters the adder 15 displaced one row to the right, enters the adder 14 displaced two rows to the right, etc. until it enters the adder 4 displaced 12 rows to the right. If the row displacer D is in action the numerical picture enters the adder 15 displaced 13 rows to the right, the adder 14 displaced 14 rows to the right, etc. until it enters the adder 4 displaced 24 rows to the right.

Here the value $|P_i - P_j|$ or $|P_i - P_j| - 12$ will enter the selective decoder according to the state of the row displacer D. From this input information, the selective decoder forms two dominating signals. The first carries out the addition

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in the adder of the comparator of multiples into which the two pictures have been brought with their row displaced correctly relative to each other. This sum X'_k has already the correct sign of the result Z_k. If one of the two additions is zero or if in its absolute value the difference of the exponents $|P_i - P_j| \geq 24$, the numerical picture of the greater addition remains intercepted in the adder 3, from which it is taken unchanged by the selective decoder. The second signal, coming from the selective decoder, opens to the formed sum X'_k the path to the searcher of boundaries. The absolute value of the sum passes through it to the conductor R, and then, via the router W and the conductor H, back to the input of the adder 15.

At the same time, the sign digit Z_k is formed, which is sent by the conductor Z to the sign memory ZP.

In the case of operation S (addition with correction) or operation SM (subtraction with correction) the adder 15 produces correction of the sum X'_k. In the case of operation ST (addition without correction) or SMT (subtraction without correction) the sum is arranged in such a way that the first 24 valid digits of the sum X'_k are intercepted without correction.

The sum X'_k having 25 binary places, then goes from the adder 15 to the displacer of results. In the displacer of results, the sum X'_k is displaced to the left until its first unity stands immediately after the row comma, where the numerical picture of the result X_k is obtained.

The information on the number of places by which the result has been displaced, is sent by the displacer of results via the distributor of exponents RE to the adder O_1. The adder O_1 retains the greater of the two original exponents P_i, P_j and, on the basis of the information from the displacer of results, carries out the correction of this exponent. The correction, consisting in the displacement of the numerical picture by one place to the right, occurs during its transportation from the memories VPi, VPj to the comparator of multiples. The sign of the result exponent is formed in accordance with the sign of the difference $P_i - P_j$, as already

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explained.

At this point the exponent P_k is ready in the subtractor O_1. The subtractor investigates whether the value of the exponent which lies in the range of $-31 \geq P_k \geq 31$. If P_k satisfied this condition, it is sent at the proper moment via the switch of the output of exponents PVE to the output conductor of the operational unit, that is, always in its absolute value and provided with the corresponding sign. At the same time the numerical picture X_k is sent from the displacer of results to the output conductor and from the sign memory ZP to the sign Z_k. The numbers X_k, P_k, Z_k form the word which depicts the resultant sum according to code B.

If the value of the exponent $P_k > +31$ the adder O_1 sends the corresponding signal via the switch of the output of exponents PVE to the verifier of operation, which transmits it to the control. The signal announces that the result is greater than the greatest number depicted according to code B.

If the value of the exponent $P_k < -31$, the adder O_1 sends to the output conductor of the operational unit $P_k = 0$ and at the same time enables the sending of $X_k = 0$ and $Z_k = 0$.

If the resultant numerical picture X_k comes out zero, the displacer of results sends to the output conductor of the operational unit $X_k = 0$ and at the same time enables the sending of $P_k = 0$ and $Z_k = 0$.

Figure 4.2 represents a simple example of the course of operation SM, that is, for example, where $|P_i - P_j| < 12$. The course of operation S where $|P_i - P_j| \geq 12$ is represented in Fig.4.3. In both figures, for the sake of simplicity, only some of the adders of the comparator of multiples are indicated.

4.5 <u>Multiplication</u>.

Operation marks:

N	Multiplication with correction
NT	Multiplication without correction

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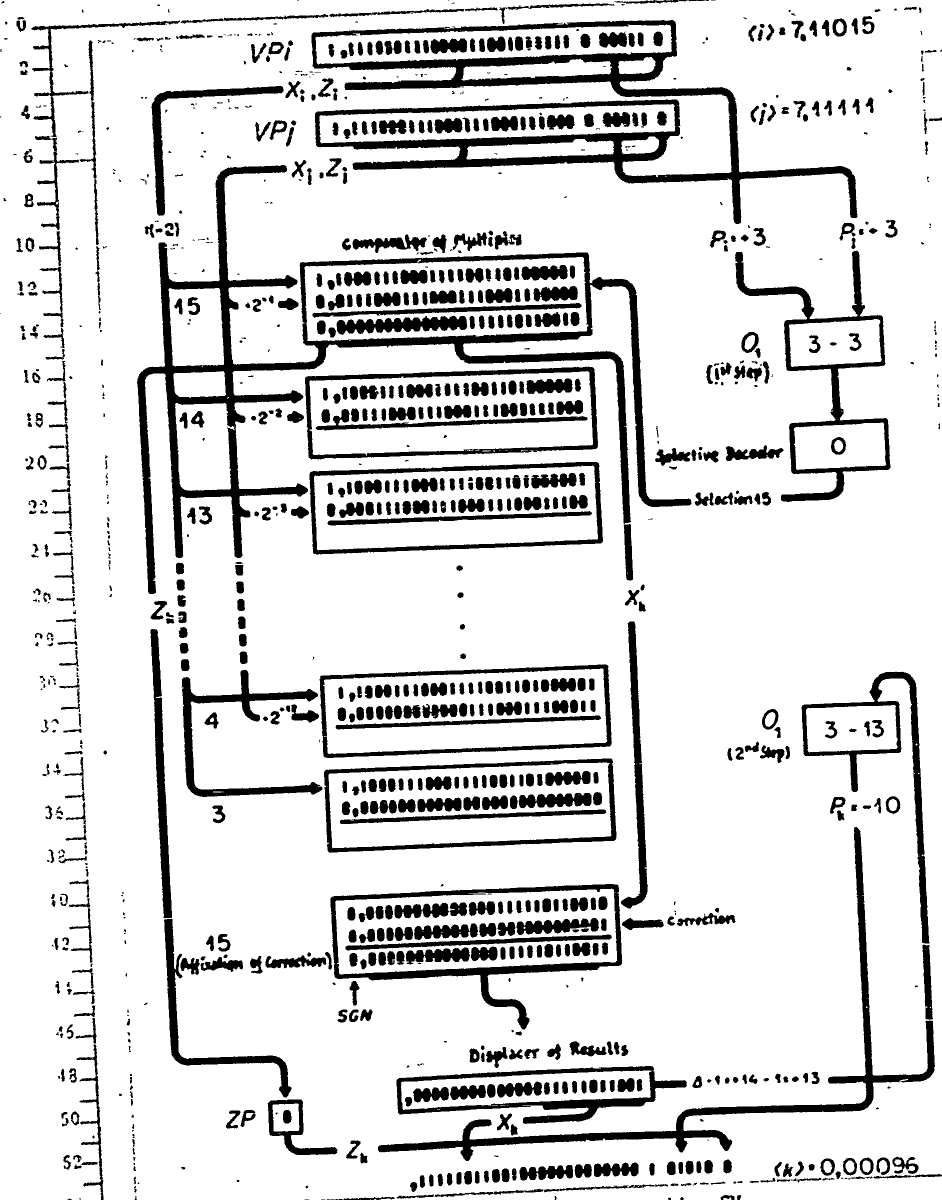

Fig.4.2 - Example of Course of Operation SM

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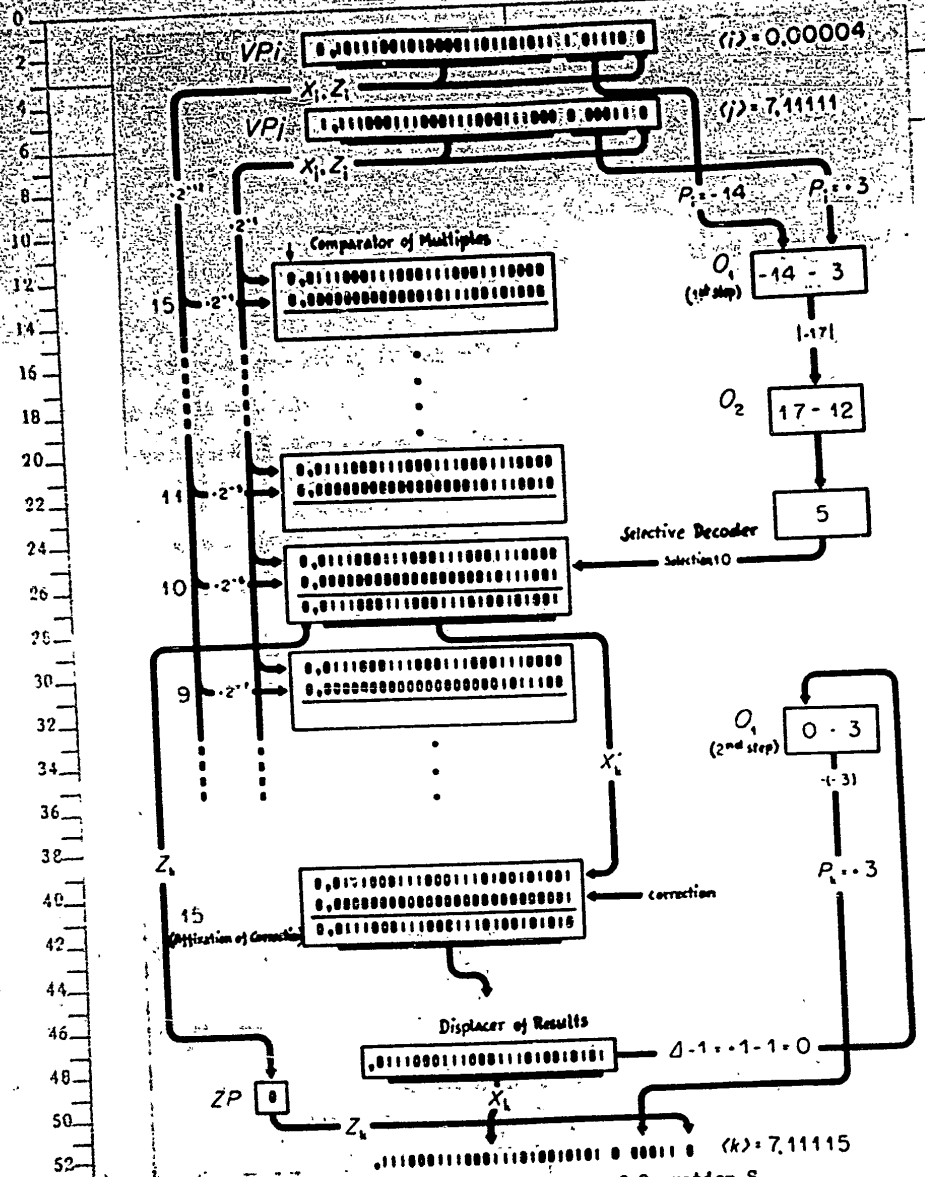

Fig.4.3 – Example of Course of Operation S

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Mathematical Principle of Multiplication. At the selection of the mathematical principle of the multiplication it was necessary to fulfill two fundamental requirements. On the one hand the adopted principle had to enable utilization of a part of the universal operational unit and on the other it also had to be satisfactory with respect to the temporal duration of the operation. From this there followed the necessity of arranging the multiplicands and multipliers in the manner described below.

From the numerical picture X_j of the multiplicand we calculate the single multiple, the double multiple, etc. until the 16-fold multiple of each of the 16 values X_j. From these 16 multiples we form the resultant sum in the manner described below.

In the numerical picture X_i the multiplier, which has 24 binary places, each five digits are denoted by the letters c_i ($i = 1, 2, 3, 4$) according to the formula

$$, \cdots c_4 \cdots c_3 \cdots c_2 \cdots c_1 \cdots$$

The picture is then divided, beginning at the right, into groups of five digits each. The last group on the left, which if four-digital, is supplemented with zero to five-digital:

$$0 \cdots c_4 \cdots c_3 \cdots c_2 \cdots c_1 \cdots$$

The value of each of these five-fold digits is in the range of 0 to 31. Each of the five-fold digits therefore represents one digit in a 32-fold system. We have therefore the original picture X_i written in the form of five 32-fold digits.

If we had at out disposal the simple, double, etc until the 32-fold multiplicands we could select according to the individual five numbers the corresponding multiples and by their addition form the resultant sum.

However, we have available only the positive and negative simple, double, etc. until the 16-fold values $X_j/16$.

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In order to get along with these multiples we carry out the transformation of the individual five numbers*. For this purpose we arrange the individual five numbers with their index digits below each other according to the formula

$$
\begin{array}{l}
0\ldots\ldots \\
\quad c_4\ldots\ldots \\
\qquad c_3\ldots\ldots \\
\qquad\quad c_2\ldots\ldots \\
\qquad\qquad c_1\ldots\ldots
\end{array}
$$

The transformation begins with the five numbers the nearest to the right. The digits of c_1 must be separated. The remaining four numbers are sought in Column A of the Table of Fig.4.4. If $c_1 = 0$, we read off in column B the numbers giving the corresponding multiples of the values $X_j/16$, which are taken as the partial multiples for the formation of the resultant product. If $c_1 = 1$, the partial multiples are determined by the numbers in column C.

We now proceed to the transformation of the second five numbers from the right. We must again separate the digits of c_2. To the remaining four numbers we add the lowest row of digits c_1. The resultant four numbers are again sought in column A of the Table. We proceed further as follows:

a) $c_2 = 0$, transferred to the affix c_1 does not come from the four numbers; in this case we select the multiples according to column B;

---

* The course of the transformed multipliers is similar to the familiar multiplication with cancellation. If the value of the five numbers is greater than 15, the next higher five numbers is increased by unity (and hence by 32 with respect to the considered five number), and the considered five number is replaced with the number which when subtracted from 32 gives the original value of the five number. This replaced number is always in the range of -1 to -16.

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b) $c_2 = 1$, transferred to the affix c_1 does not come from the four-number; in this case we select the multiples from column C;

A	B	C	D
0000	0	—16	+16
0001	+1	—15	—
0010	+2	—14	—
0011	+3	—13	—
0100	+4	—12	—
0101	+5	—11	—
0110	+6	—10	—
0111	+7	—9	—
1000	+8	—8	—
1001	+9	—7	—
1010	+10	—6	—
1011	+11	—5	—
1100	+12	—4	—
1101	+13	—3	—
1110	+14	—2	—
1111	+15	—1	—

Fig.4.4 - Table for Determination of Multiples of Values $X_j/16$ According to Four-Numbers of Transformed Multipliers

c) $c_2 = 0$, transferred to the affix c_1 comes from the four-number; in this case we select the multiples according to column C and in the group next to the left we add unity in the lowest row;

d) $c_2 = 1$, transferred to the affix c_1 comes from the four-number; in this case we select the multiples according to column B.

Then we transfer in the same way the third and fourth five-numbers.

The fifth (highest) five-number always has zero as the left end digit. At its transformation therefore, only two cases can occur:

a) transferred to the affix c_4 (or unity in the above case c) does not come from

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the four-number to the left end place (at addition of zero); in this case we select the multiples according to column B;

b) transferred to the affix c_4 (or unity in the above case c) comes from the four-number to the left end place; in this case we select the multiples from column D.

The individual partial multiples of the resultant product are added in such a way that each of them belonging to the given five-number is displaced five places to the left relative to the multiple belonging to the five-number next below.

Since the numerical value of the picture X_i is in the range of $2^{-1} \leq X_i < 2^0$ and similarly $2^{-1} \leq X_j < 2^0$, the numerical value of the product of the two pictures (or the resultant sum of all of the partial multiples) is limited to the value of $2^{-2} \leq X'_k < 2^0$, where $X'_k = X_i \cdot X_j$.

The resultant product X'_k of the pictures may therefore have its first unity at either the first or the second place after the order comma. If it has its first unity at the first place after the order comma, then X'_k represents the numerical picture of the result X_k. If, however, the first unity is at the second place, then the order of X'_k must be displaced one place to the left and the corresponding correction of the exponent carried out.

In the first case, therefore, the first 24 places of the sum of the partial multiples are used for the formation of the result and in the second case the first 25 places of the sum. The constant, with which the result has already been corrected, was determined in such a way as to avoid the occurrence of a systematic error in the result. The correction is made by affixing the binary number $I,IOL \cdot 2^{-26}$ to the resultant sum (and hence before the corresponding displacement of the order of X'_k).

For determining the exponent P_k, we first calculate the sum of $P_i + P_j$. If the sum X'_k of all of the partial multiples has its first unity at the first place after the order comma, then $P_k = P_i + P_j$. If, however, the first unity is at the

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second place, then $P_k = P_i + P_j - 1$.

The sign of the result Z_k is determined according to the rules of algebra.

Multiplication Process in Operational Unit. The binary numerical picture of the multiplicand X_j is sent from the input memory VPj by the conductor N to the input of the adders 1 to 3 of the comparator of multiples. The comparator forms and retains in its memory the simple, double, etc until the 16-fold values $X_j/16$.

The binary numerical picture of the multiplier X_i is sent from the input of the memory VPi to the transformer of multipliers. The transformer of multipliers decomposes the picture X_i into individual five-numbers and transforms these five-numbers according to the described rules. Beginning with the row of the highest group, the transformer then sends a signal which opens to the selected multiples of the values $X_j/16$ the path to the searcher of boundaries. The multiples are provided with their corresponding signs and after departing from the searcher of boundaries go from the memory of the comparator to multiples to the conductor R and via the router W to the result saver. At the same time the individual parts of the result return from the output of the result saver back to its input by the conductor of the return connection ZPV_2. The conductor of the return connection is connected in such a way that the partial sums at each passage through this conductor are multiplied by the constant 2^5 (or displaced five places to the left).

In the case of operation N (multiplication with correction) the result saver enters at the same time with the first partial multiple and the first-mentioned correction constant.

At the same time the exponents P_i and P_j are processed. The exponent P_i is sent from the memory VPi via the distributor of exponents RE to the input of adders S_1 and S_2. The exponent P_j is sent from the memory VPj, although the distributor of exponents RE has opened to it the path to the negative input of the subtractor O_1. In the latter the exponent is on the one hand retained and on the other hand sent with the opposite sign (and hence with the original sign of the

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exponent P_j) to the input of the adder S_1. In this adder, the sum of $P_i + P_j$ is then calculated and retained in its memory.

In the positive input of the subtractor O_1 the constant + 1 has in the meantime been stored. The subtractor then forms the difference $1 - P_j$. This value is sent negatively (and hence as $P - 1$) to the input of the adder S_2, where, together with the first-stored value P_i, it gives $P_i + P_j - 1$.

After all of the partial multiples have been added, the result saver signals the position of the first unity of the result X'_k. According to the position of the first unity of the sum X'_k, the exponent P_k corresponds to the picture X_k in either the adder S_1 or S_2. According to the signal of the first unity, the switch connects the output of exponents PVE of the output conductor of exponents from the operational unit with the output of the corresponding adder S_1 or S_2.

If, however, the first unity is at the second place after the order comma, the corrector of displacements Q comes into action at the same time. The number X'_k passing through the latter is in this case displaced one place to the left (or is multiplied by two). At the same time the number of binary places of the result is limited to 24. Then the numerical picture of the result X_k is obtained.

The sign of the result Z_k is formed directly in the output memories VPi and VPj. It is sent from the operational unit at the same time with the exponent P_k and with the numerical picture X_k.

Before the triple number X_k, P_k, Z_k is sent to the output conductors, the adder S_1 or S_2 tries the magnitude of the exponent P_k. If the value of P_k is not in the range of ± 31, the operation proceeds further as at addition (see paragraph 4.4), although the corresponding adder S_1 or S_2 gives the impulse to this.

If the multiplicand or the multiplier (or both) are zero, the operational unit sends positively to the output conductor $X_k = 0$, $P_k = 0$, $Z_k = 0$.

Figures 4.5 and 4.6 represent simplified examples of the course of operations N and NT. In both figures only the contents of some of the memories of the comparator

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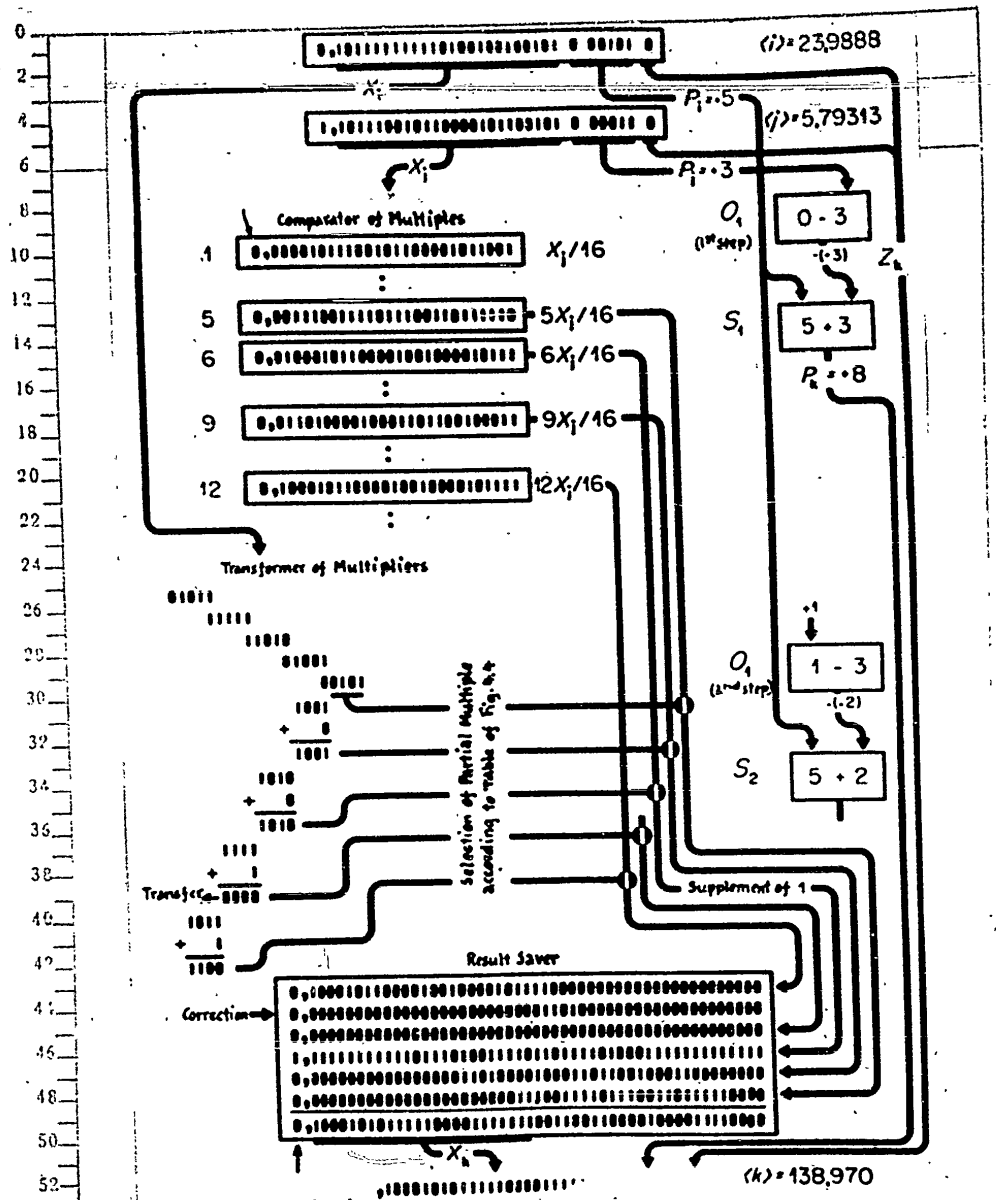

Fig.4.5 - Example of Course of Operation N

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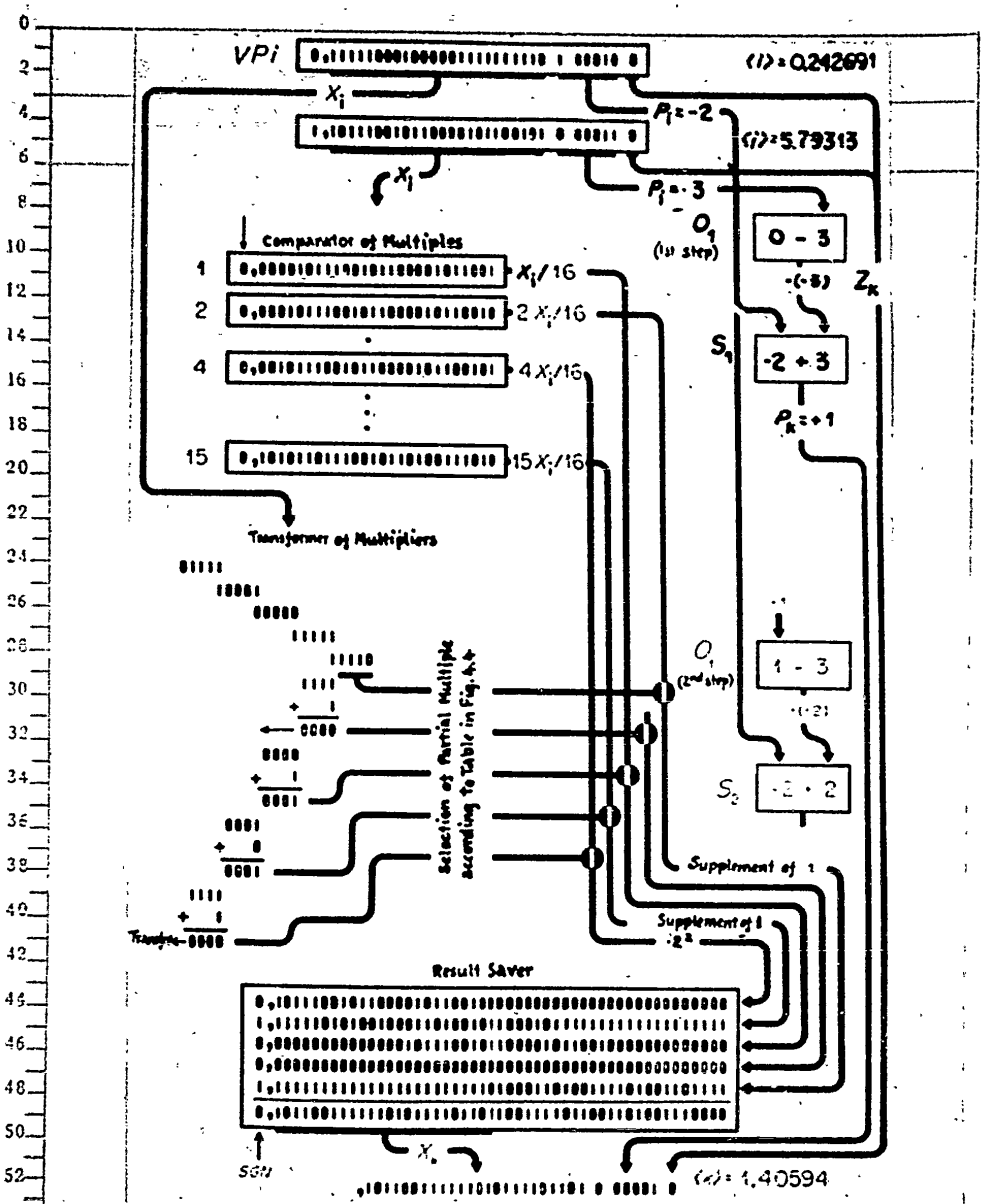

Fig. 4.6 - Example of Course of Operation NT

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of multiples are indicated. For the sake of simplicity the number of places of these memories is reduced to 26.

4.6 Division.

Operational marks:

D	Division with correction
DT	Division without correction

Mathematical Principle of Division. From the numerical picture of the divisor X_j the single etc. to the 15-fold values $-(X_j/16)$ are formed.

The numerical picture of the dividend is divided (for the reason explained below), and we calculate the 15 remainders:

$$Z_1 = \tfrac{1}{2}X_i - \tfrac{1}{16}X_j.$$
$$Z_2 = \tfrac{1}{2}X_i - \tfrac{2}{16}X_j.$$
$$\vdots$$
$$Z_{15} = \tfrac{1}{2}X_i - \tfrac{15}{16}X_j.$$

From these remainders we select the least positive remainder. The index of the remainder, expressed in the binary system, is the first (highest order) four-number quotient. We multiply the remainder by the constant 2^4 (that is, displace it four places to the left), so that all of the equations are at the place of the value $X_i/2$, and we calculate the next remainder. From them we again select the least positive remainder, which we multiply by the constant 2^4, and again add to the equation. Its index, expressed in the binary system, is connected to the second four-number of the quotient with the first four-number. This procedure is repeated six times in all. Here we obtain the 24-place binary number $X'_k = X_i/2X_j$.

The first unity in the number X'_k may be in the first or the second place after the order comma, as can easily be shown: The binary numerical picture X_i has the value $X_i = 0.1\ldots$, or, in the decimal system, $X_i = 0.5 + \delta$, where $0 \leq \delta < 0.5$;

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similarly, the binary numerical picture X_j has the value $X_j = 0.I \ldots$, or, in the decimal system, $X_j = 0.5 + \varepsilon$ where $0 \leq \varepsilon < 0.5$. Since the calculation of the quotient X_k' is carried out with the value $X_j/2$, X_k' has as its upper limit the value

$$\frac{X_i}{2X_j} = \frac{0.5 + \delta}{1 + 2\varepsilon} < \frac{0.5 + 0.5}{1} = 1.$$

The lower limit value of X_k' is

$$\frac{X_i}{2X_j} = \frac{0.5 + \delta}{1 + 2\varepsilon} \geq \frac{0.5}{1 + 1} = 0.25.$$

X_k' is therefore in the range of $1 > X_k' \geq 0.25$, or, in the binary system, $I.0 > X_k' \geq 0.0I$.

If X_k' has the first unity at the first place after the order comma it already represents the numerical picture of the quotient X_k. If it has the first unity at the second place after the order comma, we get the picture of X_k by displacing X_k' one place to the left.

For determining the result exponent P_k, we calculate first the difference of the exponents $P_i - P_j$. It will be recalled that the calculation of X_k' was carried out with the value $X_j/2$. If, therefore, X_k' has the first unity at the first place after the order comma, it is necessary to increase the exponent by +1, so that the result exponent $P_k = P_i - P_j + 1$. If X_k' has the first unity at the second place after the order comma, the exponent is likewise corrected by displacing the number X_k' one place to the left, so that $P_k = P_i - P_j$.

In view of thw fact that we have at out disposal only 24 digits of the result, we are unable to carry out the correction of the result in the usual way. With regard to the further digits of the result it should be noted that the 24th digit of the numerical picture X_k is always replaced with unity. Here an average error of $\pm 2^{-35}$ is permissible, so that the systematic error of the quotient is zero.

The quotient which comes out at 24 places without a remainder, however, is left

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without correction.

The sign Z_k of the resultant quotient is determined according to the familiar algebraic rule.

Process of Division in the Operational Unit. The numerical picture of the divisor X_j goes from the input memory VPj by the conductor N to the inputs of the adders 1 to 3 of the comparator of multiples. The comparator forms the simple, double, etc to the 15-fold values $-(X_j/16)$. These multiples are retained in the right inputs of its 15 adders, ready to be added wiht the value $X_j/2$, which enters the comparator later. Thus in adder 1 the value $-(X_j/16)$ is ready, in adder 2 the value $-(2X_j/16)$, etc.until in adder 15 the value $-(15X_j/16)$ is ready for addition. These numbers remain in the inputs of the adders during the whole operation.

The numerical picture of the dividend X_i goes from the memory VPi via the cross switch J to the conductor S, the router W and by the conductor M to the left inputs of all 15 adders of the comparator of multiples. Upon entering the comparator the picture X_i is displaced one place to the right (or is divided by two).

The comparator calculates the remainders Z_1 to Z_{15}, as already explained. The conductor A signals the signs of the individual remainders to the searcher of boundaries. At this the searcher of boundaries sets the signal in such a way that it connects the path from the comparator to the conductor for the least possible remainder. This remainder goes from the searcher of boundaries to the conductor R via the router W and by the conductor M back to the input of the comparator at the place of the value $X_i/2$. Here it is multiplied by the constant 2^4 (that is, is displaced four places to the left). The searcher of boundaries forms and sends by means of the conductor C the first four-number of the quotient to the result saver. The value of this four-number is equal to the index of the least positive remainder. The comparator again calculates the remainders Z'_1 to Z'_{15}. The searcher of boundaries again select from them the least positive remainder, and sends it to the inputs of the comparator. At the same time it sends the second four-number of

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the quotient to the result saver. This second four-number is combined with the first.

If all of the remainders Z_1' to Z_{15}' are negative, the searcher of boundaries sends out a zero four-number. In the corresponding memory, the least positive remainder of the preceding remainders Z_1 to Z_{15} is retained. The searcher of boundaries selects this remainder and sends it to the left inputs of the adders of the comparator. Here the remainder is multiplied by the constant 2^4.

After six repetitions of this process the quotient $X_k' = X_i/2X_j$ is present in the result saver. If the first unity of this quotient is at the first place after the order comma, then X_k' equals the picture X_k of the resultant quotient. If, however, the quotient X_k' has its first unity at the second place, then it must be displaced one place to the left, which the corrector of displacement Q carries out according to the signal of the result saver.

Simultaneously with the calculation of the picture X_k the calculation of the exponent P_k proceeds in the operational unit. The exponent P_i goes from the memory VPi via the distributor of exponents RE to the adders S_1 and S_2.

The exponent P_j goes from the memory VPj, likewise via the distributor RE which, however, opens the path for it to the negative input of the subtractor O_1. In the latter the exponent is on the one hand retained and on the other hand sent as $-P_j$ to the input of the adder S_2. In this adder, the difference $P_i - P_j$ is formed and is retained in its memory.

In the meantime, the constant +1 has been stored in the positive input of the subtractor O_1. The adder forms the difference $1 - P_j$. This value is sent to the input of the adder S_1, where it is combined with the first-stored value P_i with formation of $P_i - P_j + 1$.

According to the position of the first unity of the quotient X_k', the exponent P_k corresponding to the picture X_k will be in either the adder S_1 or S_2. The result saver signals the position of the first unity of the quotient X_k' to the

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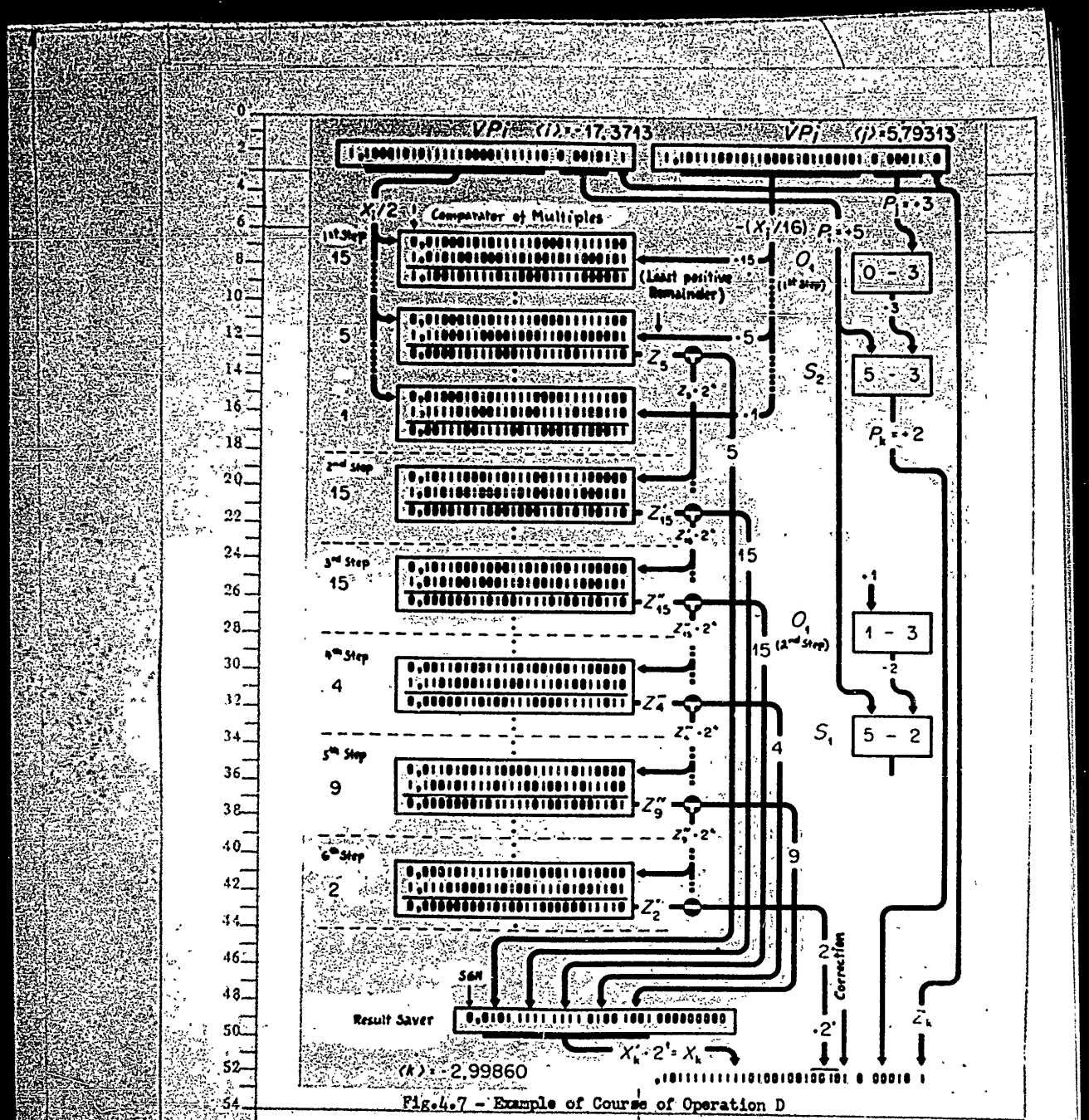

Fig.4.7 - Example of Course of Operation D

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switch of the input of exponents PVE. According to this signal, the switch PVE selects either the adder S_1 or S_2, and connects its output with the output conductor of the operational unit.

The numerical picture X_k of the quotient then goes via the corrector of displacements Q to the output conductor of the operational unit simultaneously with the selected exponent P_k. At the output of the picture X_k its 24th digit is always replaced with unity (correction). It should be noted that if the quotient comes out without a remainder we use the operational mark DT (division without correction). Simultaneously with X_k and P_k, the sign of the result Z_k also comes out and is formed directly in the input memories VPi and VPj.

Before sending the triple number X_k, P_k, Z_k to the output conductor the ada adder S_1 or S_2 verifies the magnitude of the exponent P_k. If the value of P_k is not in the range of ± 31, the further events proceed similarly as at addition (see paragraph 4.4), although the impulse to it is given by the corresponding adder S_1 or S_2.

If the dividend <i> is zero, the operational unit sends positively to the output conductor $X_k = 0$, $P_k = 0$, $Z_k = 0$.

If the divisor <j> is zero, the operational unit signals the error to the control through the intermediary of the verifier of operations.

Figure 4.7 represents in simplified form an example of the course of operation D. In the 2nd to the 6th steps only those adders of the comparator of multiples are indicated which give the least positive remainder. For the sake of simplicity the number of places of the adders of the comparator is limited to 26. For this reason, only the contents of the memories of the result saver are indicated.

4.7 Transformation.

Operational mark: T Transformation

The automatic calculator carries out the calculation only of the numbers de-

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picted according to code B (that is, in the binary system). The numbers stored in the machine in code D (that is, in the binary system) can be transformed to code B before the actual calculation. After the end of the calculation, the machine retransforms the result to code D.

In the following the denotation TL will be used for the transformation of the numbers from code D to code B and for the transformation from code B to code D the denotation T2.

The transformation of the numbers must, before carrying out operation T, be arranged in such a way as to satisfy the requirements described in paragraphs 4.8 and 4.9. The arrangement of the numbers is carried out by the machine automatically according to the instructional network, as described in (Bibl. 3).

When the operational mark T enters the memory of operational marks, the memory of operational marks verifies the contents of the memories VPi and VPj. If the contents of the memory VPj is zero the memory of operational marks connects with the proper place of the operational unit pulses which carry out the transformation of the number in the memory VPi from code D to code B, that is, the transformation T1. If, on the contrary, the content of the memory VPi is zero, then in the memory VPj the transformation of the number from code B to code D, that is, the transformation T2 is carried out. If, due to some error, the contents of both memories are not zero, the operational units carries out the transformation T2, but signals the defect to the control through the intermediary of the verifier of operations*.

4.8 Transformation T1. Mathematical Principle of Transformation T1. The word depicting the number N according to code D is formed by three numbers Y, Q, Z, at which there is valid $N = (-1)^Z \cdot T \cdot 10^Q$, where $10^{-1} \leq Y < 10^0$, $Q = 0$,

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* If the contents of both memories are zero the operational unit always carries out the transformation of the zero in the memory VPi from code D to code B (the depiction of zero in both cases is the same - see (Bibl.[1]).

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$Z = 0.1$.* After transformation to code B, the word formed by the numbers X, P, Z is formed at which $N = (-1)^Z \cdot X \cdot 2^P$, where $2^{-1} < X < 2^0$, $P = 0, -1, -2, -3$, $Z = 0.1$ is valid.

The six decimal numbers of the picture Y are denoted $y_1, y_2, y_3, \ldots, y_6$. Each of these digits is depicted by a four-place binary number. The numerical picture T is then processed according to the transformation formula

$$\{(((y_1 \cdot 10 + y_2) \cdot 10 + y_3) \cdot 10 + y_4) \cdot 10 + y_5\} \cdot 10 + y_6 = X' \quad X' \cdot 10^6$$

The individual digits y_1 to y_6 are put in the binary system. The order comma of the number X' is displaced in such a way that the last binary digit is at the twentieth place after the order comma (or the multiplication $X' \cdot 2^{-20}$) is carried out. Then $X' \cdot 2^{-20}$ is displaced with respect to the order comma in such a way that the first unity is at the first place after the order comma. Then the resultant numerical picture X is formed. The number of places by which $X' \cdot 2^{-20}$ must be displaced is given by the value of the exponent P. The sign Z remains unchanged.

From this it follows that the resultant word formed by the numbers X, P, Z depicts not the number N but the number $N = N \cdot 10^6 \times 2^{-20}$. This result after transformation was to be multiplied by the constant $10^{-6} \times 2^{20}$ in order to obtain the number N. This is done automatically by the instructional network, as described in (Bibl. 3).

Process of Transformation T1 in Operational Unit. The decimal numerical picture Y together with the exponent Q = 0 and the sign digit Z enter the memory VPi. It is composed of six decimal digits y_1 to y_6, each of which is depicted by a four-place number in the binary system. The individual decimal digits pass in succession from the memory VPi by the conductor T to the result saver (beginning with the

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* If Q does not equal 0 the number N must be correspondingly arranged before transformation. Concerning this, see (Bibl. 3).

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highest decimal digit y_1), where their contents are read. Before attribution of each decimal digits the preceding result passes by the conductor of the return connection ZPV_2 from the output of the result saver to its input, where it is multiplied by ten (according to the above formula).

The resultant number X' is transmitted from the result saver to the displacer of results. Here X' is multiplied by the constant 2^{-21}. The reason for this is that the highest unity in the number X' lies at the 17th to the 20th place before the order comma. In order that the number entering the displacer will always have a value smaller than one, the number X' is displaced 21 places to the right. This displacement occurs in accordance with the corresponding instructional network, as described in (Bibl. 3). The displacer of results displaces the number $X' \cdot 2^{-21}$ in such a way that its first unity stands immediately to the right after the order comma. After displacement by Δ places the displacer sends the correction $\Delta - 1$ via the distributor of exponents RE to the input of the subtractor O_1.

To the output conductor of the operational unit then goes the number $N \cdot 10^6 \times \times 2^{-20}$ formed by the binary digits of the numerical picture X from the displacer of results, the exponent P from the subtractor O_1* and the sign Z from the memory VPi.

If the binary number resulting from the operation T1 is greater than the greatest number depicted according to code B, the operational unit signals this defect to the control through the intermediary of the verifier of operations.

If at the operation T1 the binary number comes out smaller than the smallest number depicted by code B, the operational unit sends automatically to its output conductor the word depicting zero.

Figure 4.8 represents in simplified form an example of the course of operation T1. For the sake of simplicity the number of places of the result saver is

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* Into the subtractor O_1 only the correction of the result displacer entered during the whole operation. Therefore the exponent P equals the correction.

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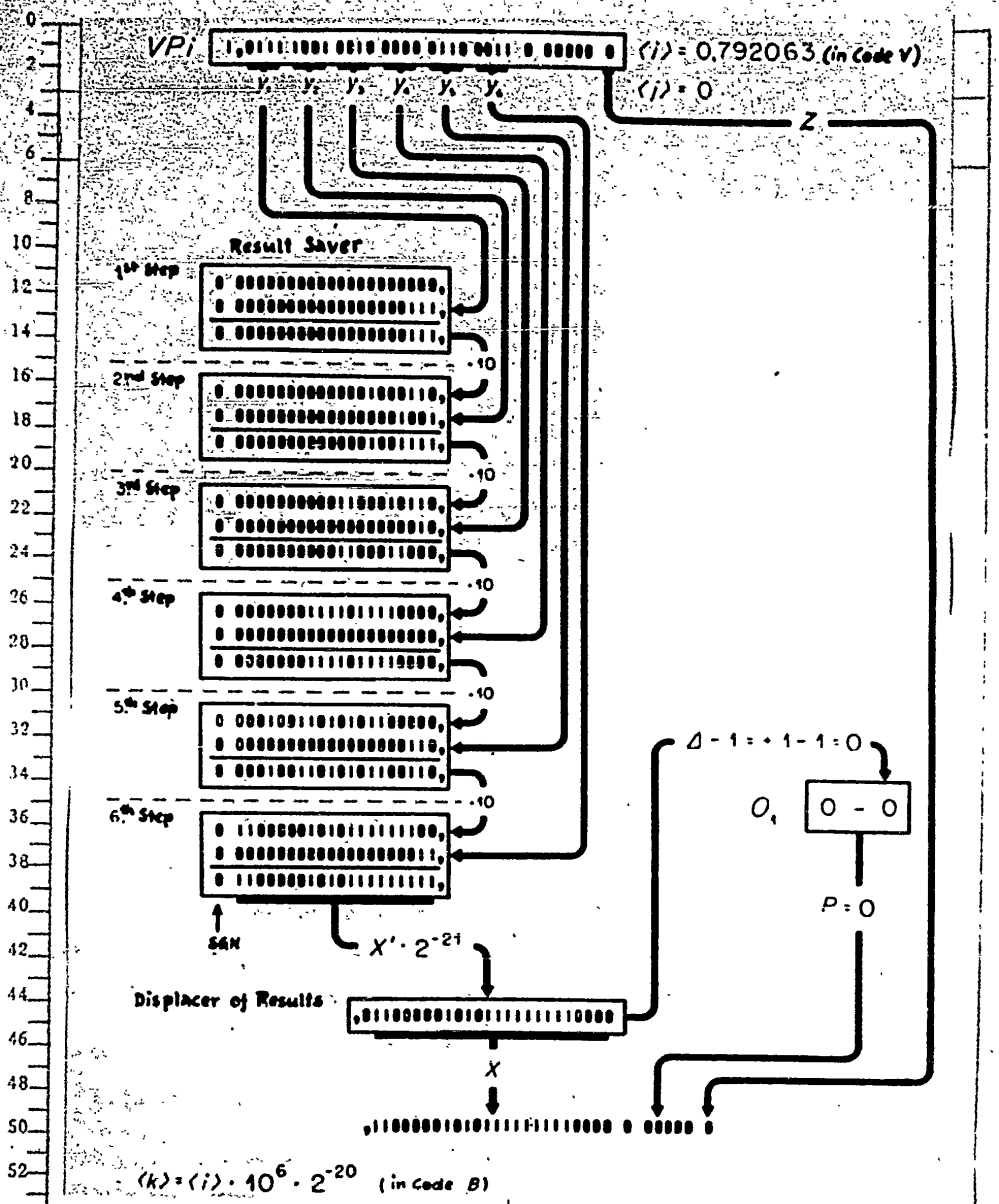

Fig.4.8 – Example of Course of Operation T1

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limited to 20.

4.9 Transformation T2. Mathematical Principle of Transformation T2. The number N depicted according to code B by the word formed by the three numbers X, P, Z is transformed to code D, in which the word formed by the numbers Y, Q, Z is depicted. To the number triplets X, P, Z and Y, Q, Z the relations described at the beginning of paragraph 4.8* apply.

The numerical picture X is displaced with respect to the order comma by the number of places to the right given by the value of the exponent P. In this way we get the number X' = (N).

Then we begin the transformation by multiplying the number X' by ten. The decimal ~~four-number~~ which after multiplication comes ahead of the order comma is separated out. This four-number already represents the binary coded first decimal digit of the decimal numerical picture Y. The binary number remaining after the order comma is again multiplied by ten, and gives the second decimal digit. The process is repeated six times in all. In this way we obtain six binary coded decimal digits composing the decimal numerical picture Y. The order comma lies immediately to the right ahead of the first decimal digit. The corresponding exponent Q is zero. The sign Z remains unchanged.

Process of Transformation T2 in Operational Unit. The binary numerical picture X together with the exponent O and the sign Z enter the memory VPj. From the memory VPj the picture X is sent via the crossing switch J by the conductor D to the right inputs of the adders 4 to 15 of the comparator of multiples. As explained in paragraph 4.4, the numerical picture entering the adder 15 is displaced one place to the right, the adder 14 two places to the right, etc, until finally the adder 4, 12 places to the right.

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* If the number P does not satisfy the condition P = 0, -1, -2, -3, then the number N must be correspondingly arranged before transformation. On this see (Bibl. 3).

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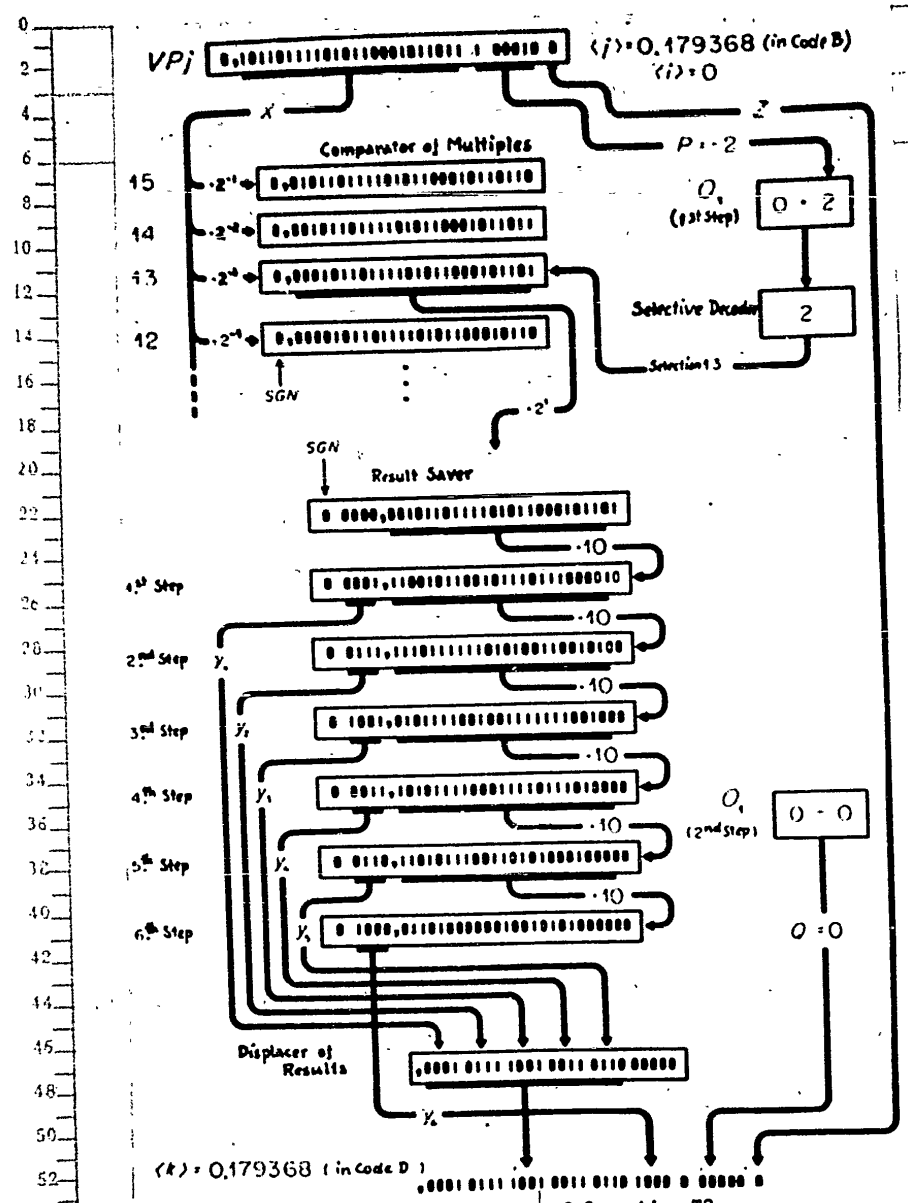

Fig.4.9 – Example of Course of Operation T2

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The exponent P_j is sent from the memory VPj by the distributor of exponents RE to the input of the subtractor O_1. From the subtractor the absolute value $|P_j|$ is sent by the row displacer D to the selective decoder.

Here the selective decoder selects the adder of the comparator of multiples in which the numerical picture X has just been displaced by the number of places corresponding to the value $|P| + 1$*. If P = 0, it selects the adder 15, if P = -1, it selects the adder 14, if P = -2, it selects the adder 13, and if P = -3, it selects the adder 12. The selective decoder opens the path to the content of the selected adder via the searcher of boundaries to conductor R and via the router W to the input of the result saver. In traversing this path the number is displaced one place to the left. At P = 0, therefore, the number enters the result saver undisplaced, at P = -1 displaced one place to the right, at P = -2 two places, and at P = -3 three places to the right.

The number passes through the result saver and upon coming out of it returns via the return connection ZPV_2 to the input of the result saver, where it is multiplied by 10. The binary four-number which after multiplication came ahead of the order comma, already represents the first (highest) decimal digit of the decimal numerical picture Y. The result saver stores this digit in the displacer of results, which is used here as a memory. The remainder after the order comma is returned from the output of the adder via the conductor of the return connection ZPV_2 to the input of the adder, and it is likewise multiplied by 10. The binary four-number ahead of the order comma represents the second decimal digit of the picture Y. The result saver is connected in the displacer of results with the first decimal digit. The process is repeated six times. Six binary coded decimal digits are formed in the displacer of results, which together form the decimal numerical picture Y. The picture goes from the displacer of results without order displacement to the output

* As mentioned in paragraph 4.8, in this case we may have P = 0, -1, -2, -3.

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conductor of the operational unit. At the same zero exponent Q and the sign Z depart from the memory VPj.

Figure 4.9 represents in simplified form an example of the course of operation T2. For the sake of simplicity, the contents of some of the memories of the comparator of multiples are indicated, with the number of places limited to 26. Likewise, the result saver has indicated only the contents of the memory in some of the individual steps; the number of places being limited to 29.

Nonarithmetical Operations

The automatic computer also carries out during its working process operations with numbers by working processes without the help of the four mathematical operations and transformations. To distinguish them from the arithmetical operations discussed in the preceding paragraphs, we call such operations nonarithmetical. Nonarithmetical operations are likewise working processes by which the machines transform instructions or forms new instructions.

4.10 Detachment of Parts of Words.

Operational marks:

SX	Detachment of exponent
SYZ	Detachment of sign
SXY	Detachment of number A
SZ	Detachment of number B
SY	Detachment of number C

In certain cases it is necessary to carry out arithmetical operations on the exponent P or Q or on the sign Z. At the transformation of instructions and the formation of new instructions, it is likewise necessary to operate arithmetically on the individual binary numbers A, B, C in the instructions. For enabling the machine to operate on such parts of words, the corresponding part is first eliminated from the remaining part of the word. To the detachment part another given number (or zero) is at the same time attached where the result is depicte

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number according to code B and stored in the central memory. The elimination, attribution and depiction according to code B are carried out in the operational unit of the machine during one working cycle.

The word on which these operations are to be carried out always enters the memory VPj via the input circular displacer. The input circular displacer is in action and brings about the circular displacement of the word (see paragraph 4.2). The displacement is governed according to which part of the work is to be detached. At this the lowest binary digit of the part to be detached always enters at the 20th place to the left in the memory VPj.

Next, the number <i>, enters the memory VPj, depicted according to code B, to be attached to the eliminated number. If the detached number comes out unchanged, the number <i> is zero.

The verifier of operations carries out unity trial in both of the input memories. After this only the part of the work to be detached remains in the memory VPj. The remaining part is forgotten.

In the negative input of the subtractor O_1 the exponent +19 (or in the subtractor -19 is present) is stored. The exponent P_i of the number <i> enters the positive input of the subtractor O_1. The subtractor calculates the difference $P_i - 19$. If the absolute value comes out $|P_i - 19| \geq 12$, the order displacer D connected with the conductor D (see paragraph 4.4) comes into action.

The absolute value of the difference between the two exponents then enters the selective decoder, that is, either directly from the subtractor O_1 or decreased by 12 from the subtractor O_2 (see paragraph 4.4). According to the sign of the difference $P_i - 19$, as at compounding, the state of the crossing switch J and hence also of the connection of the conductors D and S with the outputs from the memories VPi and VPj is determined.

Then from the memory VPi the numerical picture X_i comes out and from the memory VPj the detached number. Both pass through the crossing switch J to the in

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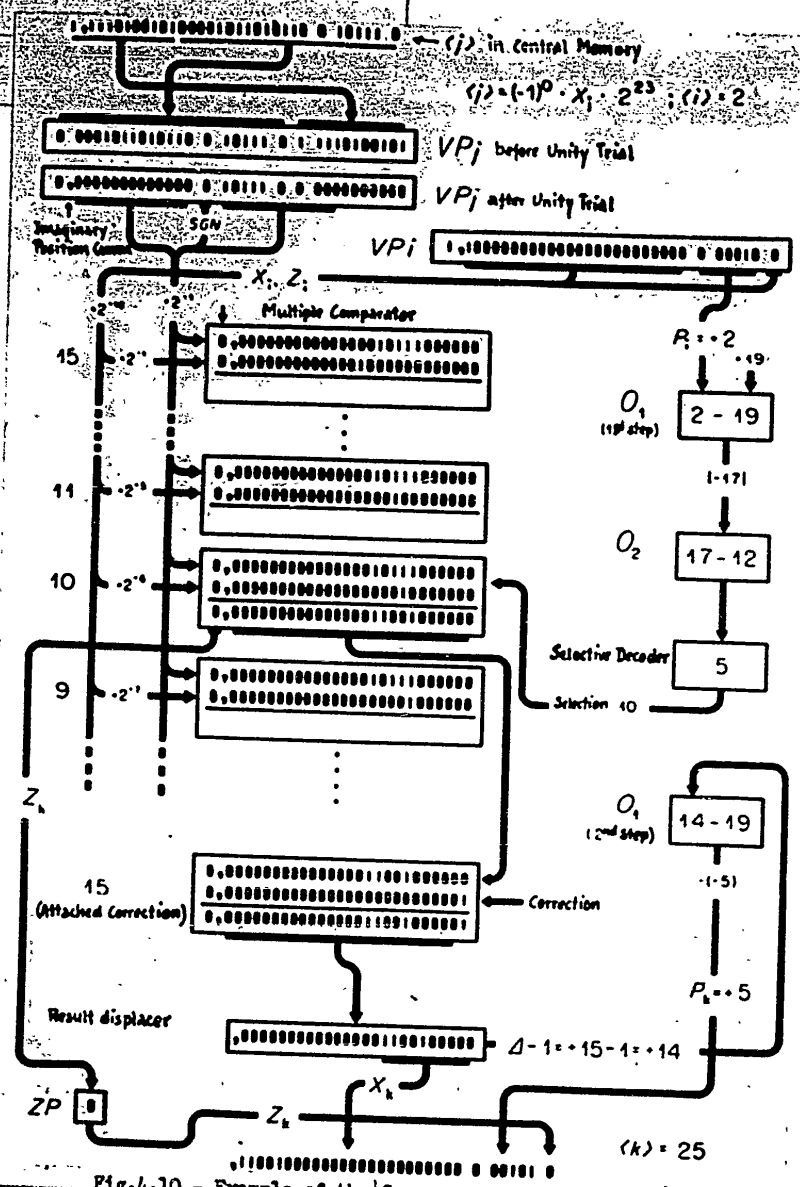

Fig.4.10 - Example of the Course of Operation SX

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of the adders of the comparator of multiples, that is, on the one hand by the conductor D and on the other hand by the conductor S via the router W. The relative position of the numbers upon adding the individual adders of the comparator of multiples is similar to that at the operation of compounding (see paragraph 4.4).

The selective decoder then opens the path to the searcher of boundaries from the adders of the comparator of multiples in which both members have been properly displaced. The absolute sum goes by the conductor R via the router W and by the conductor M back to the input of the adder 15 of the comparator of multiples. At the same time the sign digit Z_k is formed, which is sent by the conductor Z to the sign memory ZP. The adder 15 carries out the correction of the sum (the result is usually a whole number; the correction in this case is invalid). The resultant sum, having 25 binary digits, then goes from the adder 15 to the displacer of results.

In the result displacer the sum is displaced in position in such a way that the first unity stands immediately after the position comma, where the resultant numerical picture X_k is formed. Information on the number of places by which the sum had to be displaced has in the meantime been sent by the result displacer via the exponent distributor RE to the subtractor O_1. This subtractor has retained the greater of the two original exponents, and on the basis of the information from the result displacer carries out the correction of this exponent as at the operation of compounding (paragraph 4.4).

The resultant exponent P_k is now ready in the subtractor O_1, where the result displacer contains the numerical picture of the result X_k and the memory ZP contains the sign Z_k. Before this number departs from the operational unit, the subtractor O_1 verifies the magnitude of the exponent P_k, as in compounding (see paragraph 4.4).

Figure 4.10 represents in simplified form an example of the course of operation SX (detachment of exponent and attachment of +2 to its value). For the sake of simplicity only some of the adders of the multiple comparator are represented; its number of places being limited to 26.

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4.11 Replacement of Parts of Words

Operational marks:	WX	Replacement of exponent
	WYZ	Replacement of sign
	WXY	Replacement of number A in instruction
	WZ	Replacement of number B in instruction
	WY	Replacement of number C in instruction

In the preceding paragraph the detachment of certain parts of words has been discussed, which, after depiction according to code B, are stored in the central memory of the machine. The inverse of the preceding operation is the operation of the replacement of certain parts of words with numbers originally depicted according to code B. This operation (as also the operation of detachment) can be carried out on the exponent P or Q, on the sign Z of the number and on the number A,B,C in the instruction. The instruction network in which this operation is used must assure that the number which is to replace the other number in the word is a whole number, and that its magnitude does not transgress the limit given by the number of binary places of the replaced number.

The machine on which the machine has to carry out the operation enters the memory VPj. At this point it passes through the input of the circular displacer, which carries out the necessary displacement of the word in such a way that the lowest binary digit of the replaced part enters at the 20th place to the left in the memory VPj.

The number <i> enters into the memory VPi, depicted according to code B. After unity trial by the verifier the memory VPj forgets the part of the word to be replaced.

In the negative input of the subtractor O_1, the exponent +18 is stored (or in the subtractor -18 is present). The exponent P of the number <i> enters the positive input of the subtractor O_1, in which $P_i - 18$ is calculated. If the absolute value comes out $|P_i - 18|$ is not smaller than 12 the position displacer D goes into action (as at compounding; see paragraph 4.4). The difference between the exponents enters into the selective decoder as an absolute value, that is, either directly

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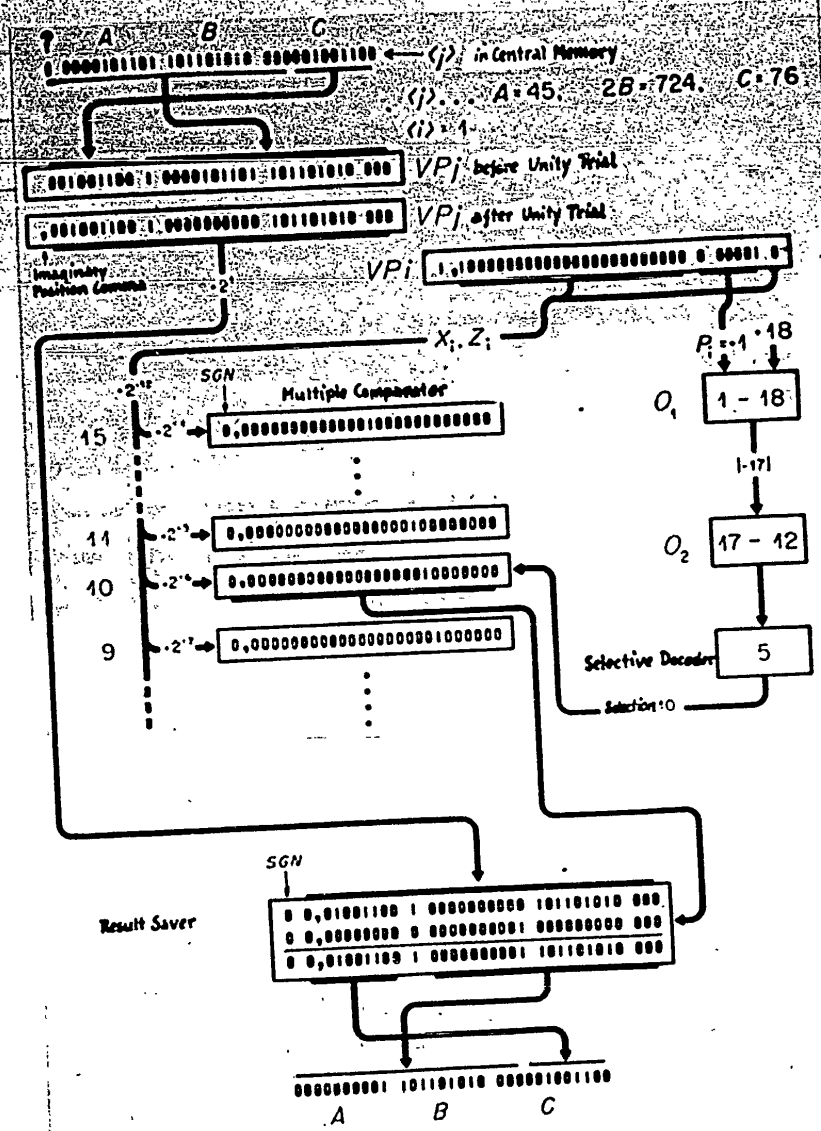

Fig.4.11 - Example of the Course of Operation WXY

a) In central memory; b) Before unity trial; c) After unity trial; d) Imaginary position comma; e) Multiple comparator; f) Selective decoder; g) Selection 10; h) Result saver

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from the subtractor O_1 or decreased by 12 from the subtractor O_2.

The greatest value of P_i may be +12, because the greater number which can be replaced is the 12-place G in the instruction. Because the sign of the difference $P_i - 18$ is always negative, the circular switch J always goes into action. Therefore, the remainder of the word always goes from the memory VPj via the circular switch J to the conductor S and via the router W to the result saver.

The numerical picture X then goes from the memory VPi via the circular switch to the conductor D and via the position displacer D to the right input of the adder of the multiple comparator. Here it is retained in the manner already described in paragraph 4.4.

The selective decoder then opens the path to the boundary searcher from the adder of the comparator in which the position of the picture X_i has been correspondingly displaced. Thus arranged, the picture X_i goes from the output of the boundary searcher to the conductor R and via the router W to the result saver.

In the input of the result saver the word from the memory VPj on which the operation is carried out is ready. The number formed by displacement of X_i in the multiple comparator enters the result saver displaced in position in such a way that the missing part of the word is correctly replaced.

With this the operation is ended, and the resultant word goes from the result saver to the output conductor of the operational unit. Then it goes to the input circular displacer, in which the same displacement of the word is carried out as in the input circular displacer but in the opposite direction.

Figure 4.11 represents in simplified form an example of the course of operation WXY (replacement of the original value of the number A = 45 in the instruction with the value A = 1). For the sake of simplicity, only the contents of some of the memories of the multiple comparator are indicated, and its number of places is limited to 26. The number of places of the result saver is likewise limited.

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4.12 Attachment to Number A, B, or C in Instruction.

Operational marks:

SWXY	Attachment to number A in instruction
SWZ	Attachment to number B in instruction
SWY	Attachment to number C in instruction

By certain operations on the instructions it is possible considerably to accelerate the operation enabling direct attachment to the number A, B or C of the instruction of a number (positive or negative) depicted by code B without its being necessary to detach the number A, B or C. At this operation the instructional network must assure that the attached number is a whole number, and that its magnitude or the magnitude of the result does not transgress the limit given by the number of binary places of the number to which it is attached in the word.

The procedure at the execution of this operation in the operational network does not differ much from the procedure described in paragraph 4.11 above.

The number <i> to be attached to the number A, B or C in the instruction is processed in the same way as described in paragraph 4.11.

The word in the memory VPj on which the machine has to carry out the operation is still intact after execution of the unity trial, and goes in this form to the result saver. The number <i> enters the result saver displaced in position in such a way that it is correctly attached to the corresponding part of the word.

The remaining events in the operational unit do not differ from the events described in paragraph 4.11

Logical Operations

A list of the logical operations which the Czechoslovakian automatic computer carries out, brief instructions thereof and of the corresponding codes, are given in (Bibl. 2). Here we shall limit ourselves to the working process in the operational unit at the execution of logical operations.

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4.13 Combination.

Operational mark: DS Combination

The words <i>, <j>, depicting logical numerical symbols, enter at the beginning of the operation the memories VPi, VPj. After execution of unity trial the symbol <i> goes from the memory VPi via the crossing switch J to the conductor S, via the switch W and by the conductor M to the input of the adder of the multiple comparator.

Simultaneously, the combination (logical addition) of the two symbols with respect to affixation of the operational marks I and J is carried out (if these marks are used), and the result goes by the conductor L to the result saver. If the operation mark K is used, the binary supplement of the logical sum is formed in the result saver. The sum is retained in the result saver until the moment when it is sent to the output conductor of the operational unit.

4.14 Penetration.

Operational mark: ND Penetration

The operational unit has connected only the circuit for the information of combinations (logical sums) of symbols. The penetration (logical product) of the symbols <i> and <j> is formed with the help of combination on the basis of the equation known from logical calculation

$$\langle i\rangle \cap \langle j\rangle = \overline{\langle \bar{i}\rangle \cup \langle \bar{j}\rangle}$$

The procedure of the operation in the operational unit is similar to that of the calculation of combinations. The only difference consists in that the operational unit forms automatically the supplemented symbols as prescribed by the above equation.

Also in this case the affixed operational marks I, J and K enable wider operational possibility in a shorter time than that necessary for the solution of logical problems.

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4.15 Supplementation.

Operational mark: KDS Supplementation

The course of the operation is similar to that of the calculation of the combination of symbols. In this case one (either) of the two symbols <i>, <j> may be zero.

Appendix

4.16 Subtraction with Help of Supplementary Numbers. With the help of supplementary numbers (4) it is possible to carry out subtraction with any adder. In the decimal system, the number which can be added to the original number for obtaining the right-hand unity in the higher order is regarded as the nine-supplement.

The 10-supplementary numbers are formed from left to right taking in succession the nine-supplement for each digit of the given number except the last, for which the 10-supplement must be taken. The 10-supplement to the number 7528 is therefore the number 2472. If, for example, we wish to subtract 7528 from the number 38,421, we write

$$38{,}421 - 7528 = (38{,}421 - 10{,}000) + (10{,}000 - 7528) = 28{,}421 + 2472 = 30{,}893$$

This process is simplified by using nine-supplements and circular transfer. Circular transfer is transfer from the highest numerical place to the lowest numerical place of the adder. The nine-supplement of the number 7528 in a six-place adder is 992,471. Here the subtraction is as follows:

```
                    038,421
                  + 992,471
circular transfer ←  030,892
                  + 000,001   ← circular transfer
                    030,893
```

If, for example, we add to the number 007,364 the number 999,999 the adder gives

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```
                  007,364
                + 999,999
                  007,363
circular transfer ←  + 001,001  ← circular transfer
                  007,364
```

Under these conditions, the operation of the adder with the number 999,999 is as with "negative zero". For this reason the nine-supplement of any number may be regarded as its negative value. The adder for n-place numbers must have n + 1 places. The highest place is reserved for the algebraic sign of the number. Zero denotes the positive sign, nine the negative sign.

The procedure at the subtraction of numbers in the binary system is similar. The only difference is that instead of nine-supplements one supplement is used.

As an example we present the subtraction of the number 5 from the number 17 in the binary system:

```
+ 17 = OIOOOI                    OIOOOI
+  5 = OOOIOI                  + IIIOIO
-  5 = IIIOIO                    OOIOII
                  circular transfer ←  + OOOOOI  ← circular transfer
                                    OOIIOO = + 12
```

5. Conclusion

Vaclav Cerny

The first design of an automatic computer for Czechoslovakia was created by Antonin Svoboda in 1947, when it was exhibited at the Badatel Institute of Mathematics of the Czech Academy of Sciences and Technologies. This design was already substantially the same as the present one.

The detailed design of the Czechoslovakian automatic calculator SAPO is the result of the work of the collective of the Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences.

The definitive design of the machine, including the mathematical principles and the original codes, was formulated in 1950 by Antonin Svoboda. He is also the

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author of the original idea of the use of light signals to some of the memory places in the central memory.

The carrying out of the selective circuit of the central memory with serial coils and the depiction of the sequence of binary numbers from 0 to $2^n - 1$ with the help of holes disposed in the form of a cubic pattern of n diaphragms were proposed by Jindrich M. Marek.

The investigation of the memory, the generator of starting impulses, the recording amplifier and the prototype of the reading amplifier were carried out by the Institute of Technical Physics of the Czechoslovakia Academy of Science according to the requirements established in April 1951 by the Laboratory of Mathematical Machines. On the basis of the results of the investigation, the Institute of Technical Physics designed the magnetic drum including the serial coils, the generator of starting impulses and the recording amplifier.

The reading amplifier was developed and formulated by the Research Institute for Electrotechnical Physics.

The detailed design of the control was formulated by Jan Oblonsky, who also improved the adpoted method of eliminating the influence of disturbances, designed the circuits for operating the machine, the circuits of the input and the output units, and their connection with the control.

The detailed design of the operational unit, including the design and connection of the circuits for carrying out nonarithmetical and logical operations, the arrangement of the original operational codes, the widening of the codes for making them more time-saving, and the formulation of the codes of the logical operations were carried out by the author of this article.

The relay parts of the machine were designed, for example, by ARITMA.

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SUMMARY

The work describes the Czechoslovak automatic computer SAPO, built by the Computation Laboratory of the Czechoslovak Academy of Science in Prague. SAPO is a relay computer with magnetic drum memory with a capacity of 1024 words consisting of 32 binary digits. It works in the binary system and is equipped with a floating binary and decimal point. Coding is described in detail in the volume "Stroje na zpracovani informaci, Sbornik I., Matematicke stroje", publ. by Czechosl. Acad. of Sci., Prague 1953. Input and output of data is through the use of punched cards, either in the binary or decimal form. The entire computer, with tripled operating units, will consist of about 7000 relays and 400 electronic valves. The computer is designed so that an accidental error originating in any part of the equipment has no influence on the correctness of the answer. The author of the basic design is Antonin Svoboda.

The introductory part gives general information on SAPO. The structure of the 5-address instruction is described, and on the basis of a very simplified schematic diagram, the function of the instrument and the principle of protection against errors are explained.

The second part describes the central magnetic memory with a capacity of 1024 words on two drums, describing the state of the work before it advanced to recording

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1024 words on one drum. The coincidence circuit which selects the required location on the drum with the aid of luminous signals and nine diaphragms is described in detail.

The third part is devoted to the control of the computer. The block diagram of the control is first given with a brief description of its circuits. The functioning of the control during the operation of the machine is then described, and the method of automatically eliminating the effects of errors is explained. In connection with the control, the functioning of the input and output units of the computer are described.

The fourth part is devoted to the universal operation unit. The block diagram of the universal operation unit is briefly described and the codes of the basic operations are looked over. The individual basic operations are then described in detail, both from their mathematical aspects and as the operations occur in the course of the functioning of the unit. In the case of more complex operations examples are given.

The fifth part roughly outlines the history of the SAPO project.

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CODES OF LOGICAL OPERATIONS WITH CZECHOSLOVAKIAN AUTOMATIC CALCULATOR SAPO

by

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Received: November 21, 1953

Introduction

Toward the end of the realization of the project of the Czechoslovakian automatic computer, the desire arose to enable the machine to solve problems of logical calculation. For this purpose, the operational unit on the one hand and on the other hand the code of the machine were supplemented. For technical reasons the part of (Bibl. 1) could no longer be supplemented relating to the codes of the automatic computer. We therefore recommend that the reader review the fundamental operations of the automatic computer described in (Bibl. 1).

Code of Logical Numerical Symbols

The automatic computer works with logical numerical symbols of 23 binary elements. The word depicting the logical numerical symbol is formed as follows:

?	0	.....	0000000
parity	blind place	numerical symbol	blind places

Of the 32 binary digits of the word 23 belong to the logical numerical symbol, at eight places there is always zero (blind places), and the remaining 32nd digit (parity) is formed in dependence on all of the remaining digits of the word in such a way that the sum of all 32 digits of the word is odd*. The individual places of the word depicting the 23-place numerical symbol are numbered from left

* Parity serves for verifying the correctness of the word transmitted to the machine.

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to right as follows:

0, 1, 2, 3, 4, etc to 22

Each of the numbers corresponds to one of the elements of the fundamental quantity I (read i) of 23 elements. The numerical symbol is then expressed by the subquantities of this fundamental quantity I, and, specifically, in such a way that from the fundamental quantity the elements lying at the places at which the numerical symbol has unity are selected. For example, the logical numerical symbol

00I00000I0II00000I0I00I

corresponds to the subquantities

2, 8, 10, 11, 17, 19, 22

of the fundamental quantity I.

In (Bibl. 2) it is shown that the logical numerical symbols are isomorphous with the Boolian algebraic expressions, and the introduced relations between the operations with the numerical symbols and the Boolian algebraic expressions follow from this isomorphy.

Codes of Instructions

The codification of the instructions on whose basis the machine carries out the solution of logical problems does not differ from the codification at the solution of numerical problems. It is published in (Bibl.1), and need not be repeated here.

Operations with Numerical Symbols and Operational Marks

The automatic computer carries out directly three fundamental operations with logical numerical symbols: combination (logical sum), penetration (logical product), and supplementation. The definitions of these operations are given in (Bibl.2).

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OOIOOOOOIOIIOOOOOIOIOOI

corresponds to the subquantities

2, 8, 10, 11, 17, 19, 22

of the fundamental quantity I.

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As is known from (Bibl.1), the machine carries out the selection of the operations according to the 12-place operational mark f_1, whose individual binary digits are denoted by letters as follows:

IJKNDSWXYZMT

In the instruction, therefore, only those elements of the operational mark f_1 which correspond to the places at which the numerical picture of the operational mark has unity are included.

Next we introduce the principal operational marks of the logical operations and their relations to the given operational marks. Of the given operational marks we use only the marks I, J, K, G, H. The meanings of the operationsl marks I, J, K at logical operations differ somewhat from their meanings at numerical operations, and are given below. The meanings of the operational marks G, H are given in (Bibl.1).

1. Principal Operational Marks.

Mark: DS Combination $\langle i\rangle \cup \langle j\rangle - \langle k\rangle$

The machine starts with the numerical symbols <i>, <j> from the memories of addresses i, j. It carries out combination (logical sum) of the two symbols. As a result the symbol k replaces the content of the memory of address k.

Mark: DS Penetration $\langle i\rangle \cap \langle j\rangle - \langle k\rangle$

The machine starts with the numerical symbols <i>, <j> from the memories of addresses i, j. It carries out penetration (logical product) of the two symbols. As a result the symbol <k> replaces the content of the memory of address k.

Mark: KDS Supplementation $\overline{\langle i\rangle} - \langle k\rangle$ at $\langle j\rangle = 0$

$\overline{\langle j\rangle} - \langle k\rangle$ at $\langle i\rangle = 0$

The machine starts with the numerical symbols <i>, <j> from the memories of addresses i, j. Here one (any) of the two symbols is zero. From the remaining non-zero symbol the machine forms the supplementary numerical symbol, which replaces

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the content of the memory of address k.

If <i> = <j> = 0, the machine forms the result <k> = I, where I is the fundamental quantity of the whole number.

2. Added Operational Marks

Marks:

I Supplementation of numerical symbol <i> $\overline{<i>}$

J Supplementation of numerical symbol <j> $\overline{<j>}$

The machine carries out the operation prescribed by the principal operational mark on the supplementary symbol $\overline{<i>}$ or $\overline{<j>}$ to the given original numerical symbol <i> or <j>. The result of the operation replaces the content of the memory of address k.

These marks are mutually nonexclusive, and can be used in combination with the principal operational marks DS, Nd, and with the added operational marks K, G, H.

Mark: K Supplementation of result <k> $\overline{\cdots}$ - <k>

At the replacement of the content of the memory of address k with the result of the operation with the given principal operational mark, the numerical symbol of the result is changed to the supplementary symbol.

This mark can be used in combination with the principal operational marks DS and ND and with the added operational marks I, J, G, H.

A survey of the operational marks is presented in the Table of Fig.1. In the first column of the Table the operational marks are given in the second column the corresponding instructional symbols in the general form, and in the third column the detailed meanings of the two words prescribing the corresponding instructions according to the instructional code. The information in the column of the general instructional symbols is arranged as follows: on the left is the address of the first half of the instruction according to which the machine carries out the operation denoted by the operational symbol in the middle; after carrying out the operation the machine proceeds further according to the instruction whose first half is

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a)		b) c)	d)			e)		
DS	LA	$\langle i \rangle \cup \langle j \rangle \rightarrow \langle k \rangle$	LB	0	LA	k	LB/2	DS
						j	0	i
ND	MA	$\langle i \rangle \cap \langle j \rangle \rightarrow \langle k \rangle$	MB	0	MA	k	MB/2	ND
						j	0	i
KDS	NA	$\overline{\langle i \rangle} \rightarrow \langle k \rangle$	NB	0	NA	k	NB/2	KDS
						0	0	i
	NC	$\overline{\langle j \rangle} \rightarrow \langle k \rangle$	ND	0	NC	k	ND/2	KDS
						j	0	0
I	PA	$\ldots \overline{\langle i \rangle} \ldots \rightarrow k$	PB	0	PA	k	PB/2	I ...
						j	0	i
J	PC	$\ldots \overline{j} \ldots \rightarrow k$	PD	0	PC	k	PD/2	J ...
						j	0	i
K	PE	$\overline{\ldots} \rightarrow k$	PF	0	PE	k	PF/2	K ...
						j	0	i

Fig.1 – Meanings of Operational Marks

a) Operational mark; b) General instruction symbol; c) Address of instruction; d) Operational symbol; e) Complete instruction

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stored at the address given at the right. The pairs of capital letters denoting the addresses are taken at random, and have no relation to the operation (for further details, see (Bibl.1).

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SUMMARY

The article supplements the 2nd chapter of the publication "Machines for Information Processing, Vol.I, Mathematical Machines", publ. by Czechosl. Acad. of Sci., Prague 1953. It describes logical operation codes which enable the Czechoslovak Automatic Computer SAPO to solve problems in the calculus of logic.

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COMPOSITION OF INSTRUCTIONAL NETWORKS FROM AVAILABLE INTEGERS

by

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Received: January 29, 1954

1. Introduction. In Collection I the method for the preparation of the instructional network is described. In this article a procedure which saves work at the preparation of the instructional network, and applicable in some cases, is described.

Assume that in several different instructional networks a part of the network by which the same problem is solved is repeated, for example, calculation of the root or calculation of the value $y = \cos x$. Recently Antonin Svoboda recommended that such partial problems be solved with stock instructional networks, to be incorporated as necessary in the extended instructional network proposed by him.

When what is concerned in the present article is an instructional network to be incorporated in a larger instructional network, it will be called the "instructional sub-network" or briefly the "sub-network".

In the second paragraph a case where a stock instructional network is incorporated in a larger network as a subnetwork is discussed, while in the fourth paragraph the standard form which any instructional subnetwork must have in order to work as simply as possible is described. In the concluding paragraph the method of employment of the subnetworks from the practical viewpoint is discussed.

2. Incorporation of Instructional Subnetwork. Assume that a sufficient number of instructional subnetworks has already been prepared in detail, and that there the packs of perforated cards in which the subnetworks are perforated are available.

Assume that for a new instructional network it is sufficient to fill out "formula 1" of the form for ascertaining whether a ready subnetwork for a certain

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type of problem is available in an existing instruction network. If it is, we designate "formula 1" of the form as merely the type of this partial problem* and let it go at that.

For filling out "formula 2" of the form, that is, with respect to the contents of the memory places** of the machine we must know the following facts regarding the instructional subnetwork:

a) We must know in which memory the input value must be stored in order for the machine to be able to process the considered subnetwork. We are, therefore, interested in the address of the input value.

b) We must know at which memory of the machine to store it for calculating the result according to the considered subnetwork. We are, therefore, interested in the address of the output value.

c) In order to be able to connect the instruction of the subnetwork with the preceding instruction of the network, we must know the address at which the first instruction of the subnetwork is stored. The address will be called the input address ***.

d) In order to be able to connect the further instructions of the network with the instruction of the employed subnetwork, we must know the address at which the machine will finally calculate according to the subnetwork of the sought further instructions. This address will be called the output address.

e) We must know which memories of the machine are already occupied by subnet-

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* For example, the subnetwork for solving this type of problem: To calculate the value $y = \cos x$ with transmission, given the number $\varepsilon = 2^{-20}$; the input value is x, the output value is y. If there is given, for example, $x = 0.4$, we speak of the problem in distinction from the type of problem.

** See the word (2)1 for avoiding confusion with the central memory we speak not of the memory place but simply of the memory.

*** Not to be confused with the address of the input value!

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works. The remaining instructions of the whole network must be such that the machine is unable to store anything further in these memories*. We are, therefore, interested in the addresses of the occupied memories.

f) We must know in which memories of the machine to store the intermediate results during the calculation according to the considered subnetwork. These memories can be used both before and after for the subnetwork, although it must be borne in mind that the machine destroys their contents while operating according to the subnetwork. The addresses of this kind will be called the transitory addresses. We are, therefore, interested in the addresses of the transitory memories.

All of the addresses enumerated under points a) to f) will be called the characteristic addresses of the subnetwork.

3. Example. In article (3), in Figs. 2 and 3, the instructional subnetworks for the transformation of numbers from the decimal to the binary system are given. Their characteristic addresses are:

a) The address of the input value is 20;

b) The address of the output value is 30;

c) The input address is 40;

d) The output address is 76 and is a part of instruction AE;

e) The addresses of the occupied memories are 0, 1, 40 to 75;

f) The addresses of the transitory memories are 21, 22, 30.

Assume that we have an instructional network in which we wish, among other things, to transform a number with the help of the considered subnetwork, we must make sure that the considered network contains the instruction according to which this number (that is, the input value of the subnetwork) is at the proper moment

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* Except for the formation of the corresponding instructions the subnetwork is unnecessary for the remaining part of the calculation.

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stored in the memory 20. In the address, with which the subnetwork must correspond, we put as the address of the further continuation the number 40 (that is, the input address of the subnetwork). After transformation according to the subnetwork the number (that is, the output value of the subnetwork) is in the memory 30. The instruction according to which the machine has to proceed further is stored at the address 76 (that is, at the output address of the subnetwork).

4. Proposed Uniform Arrangement of Instructional Subnetworks. At the simultaneous employment of several subnetworks in the same instructional network some of them might obstruct each other. This can be avoided by preparing a separate subnetwork for each type of problem and locating the latter in different groups of the memory places. From these subnetworks the suitable one is then always selected.

The proposed directions for locating the instructions and constants of the subnetwork in the memory places will now be presented. The directions apply to the preparation of the detailed instructional subnetwork at "formula 2" of the form*.

In the majority of instructional networks certain constants besides the instructions and the input values also are present, for example, π, 2 and others. The latter will be called network constants. Some of them are common to several instructional networks or subnetworks. From the network constants must be selected the 16 most frequent ones, and each of them must be assigned to one of the memories 0 to 17**. These 16 constants may be called the more frequent network constants.

An instructional subnetwork usually requires several transitory memories. These may be common to all of the instructional networks. As the transitory memories may be selected once for always the memories of addresses 20 to 37. The input and output information may also be stored in the transitory memories without hesitation.

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* The instructional networks formulated in the article (3) have the proposed arrangement.

** The addresses of the memory places are given in the octonary system.

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All of the remaining instructions and constants of the subnetwork are assigned to a series of memories whose addresses immediately follow each other, and, specifically, in such a way that the reserved memories form at "formula 2" of the form, a segment occupying half of the page or even of several pages. The segment is occupied as follows:

In its first pair of memories the first instruction of the subnetwork is placed. Then follow all of the remaining instructions except the last. The further memories are reserved for the auxiliary constants or for the input or output values (if they are not placed elsewhere). The last instruction of the subnetwork is placed at the penultimate pair of memories of the segment*. In the last pair of memories at the employment of a subnetwork, the instruction according to which the machine is to proceed further after the end of the calculation according to the subnetwork, is stored.

By the delimitation of the segment of the subnetwork in "formula 2" of the form, its input and output addresses are at the same time determined. The memories 0 to 17 may be regarded as occupied memories and further all of the memories of the segment except the last pair. The memories 20 to 37 may be regarded as transitory memories. Moreover, between the occupied memories, memories which are actually free also remain. These memories can be used as needed.

5. Conclusion. The preparation of a problem for solution on the automatic computer is easy if it is already in stock on the cards of the corresponding instructional network. If it is not in stock, much work can be saved by preparing a subnetwork. In filling out "formula 2" of the form for the new instructional network, free places necessary must be left for the characteristic addresses of the employed subnetwork. According to this form, the necessary cards are perforated and to them

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* This does not take into consideration the case where there are several successive

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are added the existing cards of the employed subnetwork.

With the procedure described in this article it is possible, among other things, to store the information in the automatic calculator SAPO in the form of perforated cards independently of the sequence in which these cards are put in. The location of the instructions in the central memory need not correspond to the temporal sequence at the calculation.

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SUMMARY

The article is concerned with the planning and coding of problems for the automatic computer. It is a continuation of work in the volume "Stroje na zpracovani informaci, Sbornik I, Matematicke stroje", publ. by the Czechosl. Acad. of Sci., Prague, 1953. It is concerned with the methodology of design of instruction nets which may be assembled from units prepared in advance.

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INSTRUCTIONAL NETWORKS FOR TRANSFORMATION OF NUMBERS IN AUTOMATIC COMPUTER SAPO

by

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Received: January 29, 1954

In this article, two instructional networks* are proposed. The first of them was formulated in detail according to "formula 2" of the form, and was given such a form so that it can be used as a subnetwork according to the article (3).

1. Transformation of Number from Decimal to Binary System. The problem: The number U expressed in code D** is given by the three numbers Z, Y and Q according to the formula

$$U = (-1)^Z \cdot Y \cdot 10^Q$$

Z is the sign digit, and we may have either Z = 0 or Z = 1;

Y is the numerical picture expressed in the decimal system, at which $10^{-1} \leq Y < 1$;

Q is the decimal exponent expressed in the binary system, and is a whole number in the range of $-9 \leq Q \leq +9$***.

The same number U is expressed in code B by the three numbers Z, X, P according to the formula

$$U = (-1)^Z \cdot X \cdot 2^P$$

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* Mathematical principle of transformation proposed by Antonin Svoboda.

** See the works [2] and [1].

*** This instructional network is invalid for numbers with exponent (cont'd next page)

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Z has the same meaning as above;

X is the numerical picture expressed in the binary system, at which $2^{-1} \leq X < 1$;

P is the decimal exponent.

As follows from (Bibl. 2), the automatic computer can solve the principal part of this problem in one working cycle. According to the operation denoted T1 the number U given in code D is calculated in the same way as the number M given in the code B, in such a way that

$$M = (-1)^{Z} \cdot Y \cdot 2^{-20} \cdot 10^{6} \qquad (1)$$

The constructive arrangement of the machine requires that before beginning operation T1, zero must be present at the place of the exponent Q. It is also necessary to calculate from the number M the sought number U. These two requirements must be borne in mind at the formulation of the instructional network.

From eq.(1) it follows that it is necessary to obtain the number M multiplied by the factor $2^{20} \times 10^{-6} \times 10^{Q}$. This factor, which depends on the number Q, is called α_Q. From the range of the number Q it follows that α_Q must acquire some decimal value. If in the memory of the machine the Table of such decimal values in code B is stored, the machine must select in dependence on the exponent Q the corresponding one, multiply it by the number M, and the problem is solved.

The instructional network in general form is present in "formula 1" of the form of Fig.1. The number U is in the memory p1. The Table of values of α_Q is in

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*** (cont'd.) Q = 10. The greatest number which this network can transform is 999,999,000. The realization of a network for processing all of the numbers depicted by code B, that is, up to 2,147,480,000 has so far been impossible because of the cost of adding the necessary two further instructions and the complication of the network.

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a)	d)	e) f)	e) g)		h)
b) U (in Code D) ; c) Operation $T1$ starts w. M ; $M \cdot \alpha_Q = U$ (in Code B) $Q = -9, -8, \ldots, 0, 1, \ldots, 9$	$0 = \langle 0 \rangle$ $1 = \langle 1 \rangle$ $U = \langle p1 \rangle$ $\alpha_{-9} = \langle m1 \rangle$ $\alpha_{-8} = \langle m2 \rangle$ . . . $\alpha_0 = \langle m10 \rangle$ . . . $\alpha_9 = \langle m19 \rangle$ $m10 = \langle n \rangle$ $U = \langle p4 \rangle$	:Q0 :Q1 :Q2 :Q3 :Q4 . . . :Q12 . . . :Q21 :Q22 AA AB AC AD AE	$0 \rightarrow \langle 0 \rangle$ $1 \rightarrow \langle 1 \rangle$ $U \rightarrow \langle p1 \rangle$ $\alpha_{-9} \rightarrow \langle m1 \rangle$ $\alpha_{-8} \rightarrow \langle m2 \rangle$ . . . $\alpha_0 \rightarrow \langle m10 \rangle$ . . . $\alpha_9 \rightarrow \langle m19 \rangle$ $m10 \rightarrow \langle n \rangle$ $\mathrm{Exp}\langle p1 \rangle + \langle n \rangle \rightarrow \langle p2 \rangle$ $\langle p2 \rangle = C: \langle AE + 1 \rangle \rightarrow$ $\rightarrow !\langle AE + 1 \rangle$ $\langle 0 \rangle = \mathrm{Exp}\langle p1 \rangle \rightarrow \langle p3 \rangle$ $T1\langle p3 \rangle \rightarrow \langle p3 \rangle$ $\langle\ \rangle . \langle p3 \rangle \rightarrow \langle p4 \rangle$	AB AC AD AE BA	AB AC AD AE BA

Fig.1 – Instructional Network in General Form for Transformation of Numbers from Decimal to Binary System

a) Analysis; b) U (in code D); c) Operation T1 starts with M; d) Vocabulary; e) Instruction; f) Index; g) Operational symbol; h) Remarks; i) The address of the factor α_0 is stored in memory n; j) The address of the required factor α_Q is in memory p2; k) Address added to instruction AE

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the memories m1 to m19. The address of the factor α_Q, as well as that of the number m10, are in the memory n. According to instructions AA and AB the machine starts with the exponent Q and calculates with its help the number M10 of the address for the factor α_Q. The latter is added to instruction AE, which multiplies by the corresponding factor α_Q the result of operation T1. Instruction AC is added before operation T1 at the place of exponent zero.

Detailed instructional networks are present in Figs.2 and 3.

2. Transformation of Numbers from Binary to Decimal System. Problem: Given the number U expressed in code B to be expressed in code D.

As follows from (Bibl. 2), the automatic computer can transform in one working cycle to code D any number whose absolute value lies in the interval J is $\langle 10^{-1}, 1)$. The operation which performs this transformation is denoted T2. If the absolute value of the number to be transformed does not lie in the interval J, then this number must be resolved into two factors in such a way that the absolute of one of the factors lies in the interval J and the other factor is a whole power of ten. The exponent of this power is the sought exponent Q of the result.

The instructional network which solves this problem is represented in the group scheme of Fig.4. The number U is in the memory p1, the exponent Q of the result is formed in the memory e. The result is stored in the memory p4. If the input value of U is zero, instruction AA puts it directly in the memory for the output value*. If U differs from zero the rest of the instructional network is valid. Instruction AB cancels the content of the memory e, which will be needed later. Instructions AC and AG select the further procedure according to the magnitude of the absolute value of the number U:

if $1 \leq |U|$ the path a (case a) is valid;

if $|U| < 10^{-1}$ the path b (case b) is valid;

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* The depiction of zero is the same in codes B and D.

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Formula 2 Page 1

Index	Address		Input Information		Variable Information	Remarks
Q0	0000	P	,00000000 0 00 0	B	= 0	
Q1	0001		,40000000 0 01 0	B	= 1	
	0002					
	0003	P				
	0004					
	0005	P				
	0006	P				
	0007					
	0010					
	0011	P				
	0012	P				
	0013					
	0014	P				
	0015					
	0016					
	0017	P				
Q2	0020		U	D		p1 20
	0021	P				p2 21
	0022	P				p3 22
	0023					
	0024	P				
	0025					
	0026					
	0027	P				
	0030	P			U	p4 = 30
	0031					
	0032					
	0033	P				
	0034					
	0035	P				
	0036	P				
	0037					

Fig.2 - Detailed Instructional Network for Transformation of Numbers from Decimal to Binary System

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Formula 2

Key	Address		Input Information		Variable Information	Remarks
AA	0040		0021 0042 SXT			
	0041	P	0020 0042 0073			
AB	0042	P	0075 0044 WY			
	0043		0075 0044 0021			
AC	0044	P	0022 0046 WYZ			
	0045		0020 0046 0000			
AD	0046		0022 0074 T			
	0047	P	0000 0074 0022			
!Q3	0050	P	,44016575 1 33 0	B	$= a_{-8}$	m1 = 50
!Q4	0051		,55022334 1 32 0	B	$= a_{-8}$	m2 = 51
!Q5	0052		,70227023 1 27 0	B	$= a_{-7}$	m3 = 52
!Q6	0053	P	,43136314 1 23 0	B	$= a_{-6}$	m4 = 53
!Q7	0054		,53765777 1 20 0	B	$= a_{-5}$	m5 = 54
!Q8	0055	P	,66763377 1 13 0	B	$= a_{-4}$	m6 = 55
!Q9	0056	P	,42270137 1 11 0	B	$= a_{-3}$	m7 = 56
!Q10	0057		,52746167 1 6 0	B	$= a_{-2}$	m8 = 57
!Q11	0060	P	,65537625 1 3 0	B	$= a_{-1}$	m9 = 60
!Q12	0061		,41433675 0 1 0	B	$= a_0$	m10 = 61
!Q13	0062		,51742654 0 4 0	B	$= a_1$	m11 = 62
!Q14	0063	P	,64323437 0 7 0	B	$= a_2$	m12 = 63
!Q15	0064		,40611156 0 13 0	B	$= a_3$	m13 = 64
!Q16	0065	P	,50753412 0 16 0	B	$= a_4$	m14 = 65
!Q17	0066	P	,63148315 0 21 0	B	$= a_5$	m15 = 66
!Q18	0067		,40000000 0 25 0	B	$= a_6$	m16 = 67
!Q19	0070		,50000000 0 30 0	B	$= a_7$	m17 = 70
!Q20	0071	P	,62000000 0 33 0	B	$= a_8$	m18 = 71
!Q21	0072	P	,76400000 0 36 0	B	$= a_9$	m19 = 72
!Q22	0073		,61000000 0 6 0	B	$= m10 = 61$	n = 73
AE	0074	P	0030 0076 N			
	0075		0022 0076 —			
	0076					
	0077	P				

Fig.3 - Detailed Instructional Network for Transformation of Numbers from Decimal to Binary System

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if $10^{-1} \leq |U| < 1$*, the path e (case e) is valid.

In case a, the number U is divided by 10 (instruction AD)**, to the content of the memory e unity is added (instruction AF), and it is investigated (again with

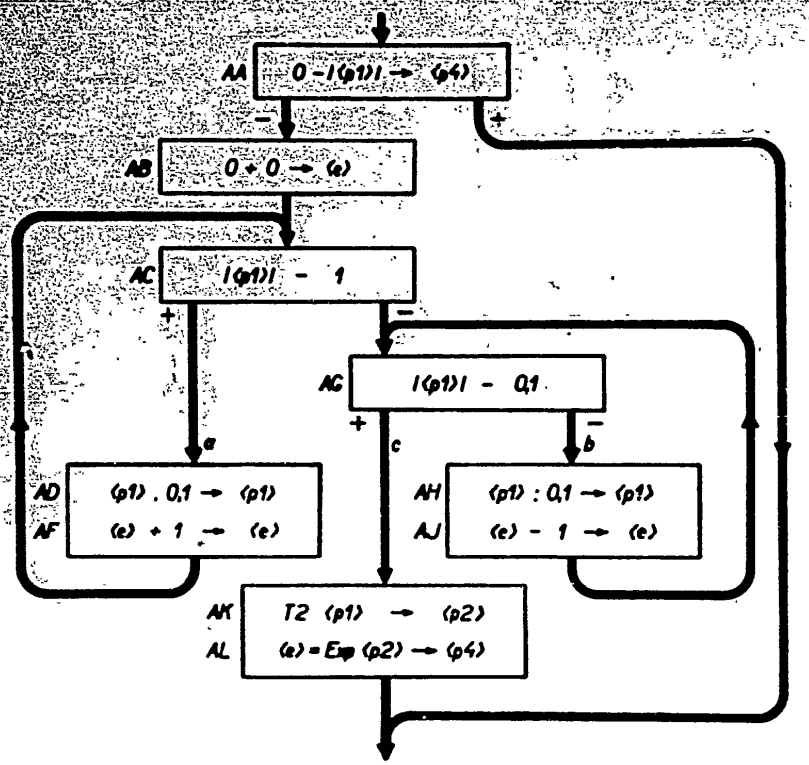

Fig.4 - Grouped Scheme of Instructional Network for Transformation of Numbers from Binary to Decimal System

instructions AC, AG) whether the absolute value of the obtained number U:10 is not already in the interval J. The procedure is repeated until the absolute value of the result of the operation AD falls in the interval J. As soon as this is the

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* (U) is in the interval J.

** Actually it is multiplied by the number 0,1.

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c)	g)	h) i)	h) j)	+	−	k)
U	$0 = \langle 0 \rangle$	!Q0	$0 \to \langle 0 \rangle$			
$U = [(-1)^z . Y] . 10^q$	$1 = \langle 1 \rangle$	!Q1	$1 \to \langle 1 \rangle$			
$10^{-1} \leq Y < 1$	$0,1 = \langle m1 \rangle$	!Q2	$0,1 \to \langle m1 \rangle$			
e) $T2$ with	$U = \langle p1 \rangle$	!Q3	$U \to \langle p1 \rangle$			
$[(-1)^z . Y]$ ↓)		AA	$-\lvert\langle p1 \rangle\rvert + \langle 0 \rangle \to \langle p4 \rangle$	BA	AB	If $\langle p1 \rangle = 0$, then $0 = \langle p4 \rangle$.
$U = [(-1)^z . Y] . 10^q$ f)		AB	$\langle 0 \rangle + \langle 0 \rangle \to \langle e \rangle$	AC	AC	
		AC	$-\langle 1 \rangle + \lvert\langle p1 \rangle\rvert \to \langle p2 \rangle$	AD	AG	
		AD	$\langle p1 \rangle . \langle m1 \rangle \to \langle p1 \rangle$	AF	AF	
		AF	$\langle 1 \rangle + \langle e \rangle \to \langle e \rangle$	AC	AC	
		AG	$-\langle m1 \rangle + \lvert\langle p1 \rangle\rvert \to \langle p2 \rangle$	AK	AH	
		AH	$\langle p1 \rangle : \langle m1 \rangle \to \langle p1 \rangle$	AJ	AJ	
		AJ	$-\langle 1 \rangle + \langle e \rangle \to \langle e \rangle$	AG	AG	
	$Q = \langle e \rangle$					
	$[(-1)^z . Y] = \langle p1 \rangle$	AK	$T2 \langle p1 \rangle \to \langle p2 \rangle$	AL	AL	
	$U = \langle p4 \rangle$	AL	$\langle e \rangle = \mathrm{Exp} \langle p2 \rangle \to \langle p4 \rangle$	BA	BA	

a) b)

Fig.5 - Instructional Network in General Form for Transformation of Numbers from Binary to Decimal System

a) Formula 1; b) Page 1; c) Analysis; d) U (in code B); e) Operation T2 starts with ...; f) In code D; g) Vocabulary; h) Instruction; i) Index; j) Operational symbol; k) Remarks; l) If $\langle p_1 \rangle = 1$, $0 = \langle p_4 \rangle$ is valid

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case, operation T2 is carried out (instruction AK). The exponent Q previously formed in the memory e is finally annexed to the result.

In case b the number U is multiplied by 10 (instruction AH), from the content of the memory e, unity is subtracted (instruction AJ), and it is investigated whether the absolute value of the obtained U · 10 is not already in the interval J. The procedure is repeated until the absolute value of the result of the operation AH falls in the interval J. As soon as this is the case, operation T2 is carried out the same as in the previous case.

In case c the start is made at once with operation T2.

The instructional network in general form is represented in Fig.5.

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SUMMARY

The article describes two instruction nets. The first system is for the transformation of numbers from the decadic system to the binary system. It is worked out in detail in table "Form 2" and is designed according to the principles presented in article [3]. The second instruction net is for the transformation of numbers from the binary system to the decadic system.

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SOLUTION OF SYSTEMS OF LINEAR ALGEBRAIC EQUATIONS BY MINIMIZATION OF SUM OF SQUARES OF RESIDUES*

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In this article a new method of solution of systems of linear algebraic equations by minimization of the sum of the square residues is proposed. The method was developed in the effort to find a universal method for the solution of systems of linear equations suitable for calculation on the automatic computer. The original method, which was presented more than a year ago by Dr.A.Svoboda to a "Conference on Machines for Processing Information", is described in Paragraph 2. The proposed new method, which considerably shortens the calculating operations carried out at the individual iterative steps, is described in paragraph 3.

1. Denotation. The system of n linear algebraic equations is written in the form of

$$Ax - a = 0$$

where

$$A = \begin{pmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & a_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ a_{n1} & a_{n2} & \cdots & a_{nn} \end{pmatrix}, \quad x = \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{pmatrix}, \quad a = \begin{pmatrix} a_1 \\ a_2 \\ \vdots \\ a_n \end{pmatrix};$$

* Presented to the Second Regular All-State Conference of the Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences in December 1953.

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the jth column of the matrix A is denoted as the vector a_j. The scalar product of the vectors $u = \begin{pmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{pmatrix}$ and $v = \begin{pmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{pmatrix}$ is denoted by the symbol $u' \cdot v$, where $u' = (u_1, u_2, \ldots, u_3)$ is the vector transposed to the vector u. The absolute value of the vector v is denoted by the symbol $|v| = \sqrt{v' \cdot v}$.

2. Description of Original Method. The given system is transformed to the system

$$Ax - e = 0, \tag{1}$$

for whose coefficient a_{ij} the following is valid

$$\sum_{i=1}^{n} a_{ij}^2 = |a_j|^2 = 1, \quad j = 1, 2, \ldots, n. \tag{2}$$

This is obtained by substitution of $\alpha_j \bar{x}_j = x_j, j = 1, 2, \ldots, n$; $\alpha_j = \sqrt{\sum_{i=1}^{n} c_{ij}^2}$, c_{ij} and x_j are coefficients or unknowns in the original system.

For the first approximation of the solution of the system (1), we take any vector $x_0 = \begin{pmatrix} x_{01} \\ x_{02} \\ \vdots \\ x_{0n} \end{pmatrix}$. Beginning with this vector we compose in succession the sequence of the vectors $x_k = \begin{pmatrix} x_{k1} \\ x_{k2} \\ \vdots \\ x_{kn} \end{pmatrix}$. The vector $x_k + 1$ is obtained from the vector in such a way that one of the components of the vector x_k, for example, x_{kl}, is changed and the other components are left unchanged. Then we put

$$x_{k+1,l} = x_{kl} - \Delta_{kl}, \quad x_{k+1,j} = x_{kj}, \quad j \neq l.$$

The value of Δ_{kl} is determined as follows: We add the vector x_k to the system (1) and obtain

$$Ax_k - e = r_k.$$

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(The components $r_{k1}, r_{k2}, \ldots, r_{kn}$ of the vector r are called the residues.) Similarly, for the vector x_{k+1} we have

$$Ax_{k+1} - a = r_{k+1},$$

at which

$$r_{k+1} = r_k - \Delta_{kl} a_l. \tag{3}$$

It is required that the sum of the squares of the residues $r_{k+1,i}$, that is, $\sum_{i=1}^{n} |r_{k+1,i}^2| = |r_{k+1}|^2 = |r_k - \Delta_{kl} a_l|^2$, be the minimum. We therefore find the value of Δ for whose function $|r_k - \Delta a_l|^2$ the variation in Δ is a minimum. This value of Δ is then taken for Δ_{kl}. For Δ_{kl}, therefore, the following must be valid

$$a_l' \cdot (r_k - \Delta_{kl} a_l) = 0,$$

i.e.

$$a_l' \cdot r_k - \Delta_{kl} |a_l|^2 = 0.$$

From this it follows with respect to eq.(2) that

$$\Delta_{kl} = a_l' \cdot r_k. \tag{4}$$

The vector x_{k+1} will therefore have as its lth component $x_{k+1,l} = x_{k,l} - a_l' \cdot r_k$.

The sequence of the vectors x_k formed in this way clearly converges the solution x of the system (1).

The sum of the squares of the residues of the kth step is increased by Δ_{kl}^2. Moreover, according to eqs.(3), (2), and (4)

$$|r_{k+1}|^2 = |r_k - \Delta_{kl} a_l|^2 = |r_k|^2 - 2\Delta_{kl} r_k' \cdot a_l + \Delta_{kl}^2 |a_l|^2 = |r_k|^2 - 2\Delta_{kl}^2 + \Delta_{kl}^2,$$

i.e.,

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$$|r_{k+1}|^2 = |r_k|^2 - \Delta_{kl}^2 \qquad (5)$$

At the kth step therefore, it is valid to calculate

$$\Delta_{kj} = a_j' \cdot r_k \qquad (6)$$

for all $j = 1, 2, \ldots, n$, and to take for l the index j for which Δ_{kl} has the greatest absolute value.

It now becomes necessary to distinguish between the selected Δ_{kl} and the remaining Δ_{kj}, so that all of the Δ_{kj} values will be called "proposed" changes and all of the Δ_{kl} values "executed changes".

In proceeding according to this method we do not calculate at each step the value of $x_{k+1,l}$ and do not obtain the new residue $r_{k+1,i}$ by annexing the vector x_{k+1} to the system (1), but instead we calculate this residue according to eq.(3). Then we determine $\Delta_{k+1,j} = a_j' \cdot r_{k+1}$ for all $j = 1, 2, \ldots, n$, i.e., also for $j = l$, which we used in the previous step. At correct calculation $j = l$ must give $\Delta_{k+1,l} = 0$.

In several iterative steps we obtain the values of the components of the last approximation in such a way that from each of the components beginning with the approximation x_o we subtract all of the "executed" changes pertaining to these components. The approximation of x_{k+1} obtained in this way is put in the system (1), by which we get the residual vector r^*_{k+1}. The vector r^*_{k+1} must with respect to the rounded error in the calculation differ from the vector r_{k+1}, which is calculated from the preceding r_k according to eq.(3). In the further iterative steps we use the vector r^*_{k+1} instead of the vector r_{k+1} and then again proceed as before. Similarly the "correction" of the residue is always carried out after several iterative steps.

If, after a certain number of steps, it is found that the sum of the squares

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of the residues is already sufficiently small (for example, smaller than that prescribed by the value ε), we stop the iterative process. We calculate the component of the last approximation and put it in the system (1), with the certainty that the residue thus obtained is sufficiently small (for example, smaller than that prescribed by the value η).

From the value x_{kj}, $(j = 1, 2, \ldots, n)$, giving the approximate solution of the system (1), we get the component $\tilde{x}_{kj}$ of the approximate solution of the given system in the form of $\tilde{x}_{kj} = x_{kj}/\alpha_j$.

3. New Arrangement of Method. At each iterative step carried out according to the method described in paragraph 2 it is necessary to determine the vector r_{k+1} according to eq.(3) and then to calculate the "proposed" change $\Delta_{k+1,j}$ $(j = 1, 2, \ldots, n)$ according to eq.(6). Each iterative step therefore requires the calculation of n expressions $r_{k+1,i} = r_{ki} - \Delta_{kl}\,\alpha_{il}$ $(i = 1, 2, \ldots, n)$ and the calculation of n scalar products $a_j' \cdot r_{k+1}$ (depending on the index k of the iterative step).

The "proposed" changes $\Delta_{k+1,j}$ can be expressed with the help of the preceding "proposed" changes Δ_{kj} and the preceding "executed" changes Δ_{kl} thus:

$$\Delta_{k+1,j} = \Delta_{kj} - \Delta_{kl}\, a_j' \cdot a_l. \tag{7}$$

From eqs.(6) and (3) it further follows that

$$\Delta_{k+1,j} = a_j' \cdot r_{k+1} = a_j' \cdot (r_k - \Delta_{kl} a_l) = \Delta_{kj} - \Delta_{kl}\, a_j' \cdot a_l.$$

The scalar product $a_j' \cdot a_j$ occurring in eq.(7) is independent of the index k of the iterative step. Hence it is sufficient, before beginning the iterative process, to calculate all of the scalar products $a_p' \cdot a_q = b_{pq}$ which can be formed from the column of the matrix A, and arrange them in the form of the corresponding Table. For the calculation of the value $\Delta_{k+1,j}$, and not before then, we selected from the elements b_{pq} the one corresponding to the value b_{jl}, and calculate

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$$_{1,j} = \Delta_{kj} - \Delta_{kl} b_{jl} \qquad (8)$$

The composition of the Table of the values of b_{pq} corresponds to the calculation of the matrix A'A (where A' is the matrix transposed to A), and it is required to calculate $\frac{n(n-1)}{2}$ scalar products. (It is clear that $b_{pp} = 1$, $b_{pq} = b_{qp}$ for all $p = 1, 2, \ldots, n$; $q = 1, 2, \ldots, n$.) Each iterative step carried out according to the method described in this paragraph comprises the calculation of only n expressions $\Delta_{kj} - \Delta_{kl} b_{jl}$, and hence gives a saving of n scalar products compared with the iterative steps carried out according to the method described in paragraph 2.

The calculation can be suitably arranged with the help of Tables B and D represented in Fig.1.

1	b_{12}	. . .	b_{1l}	. . .	b_{1n}
b_{21}	1	. . .	b_{2l}	. . .	b_{2n}
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
b_{l1}	b_{l2}	. . .	1	. . .	b_{ln}
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
b_{n1}	b_{n2}	. . .	b_{nl}	. . .	1

B

x_{01}	x_{02}	. . .	x_{0l}	. . .	x_{0n}
Δ_{01}	Δ_{02}	. . .	Δ_{0l}	. . .	Δ_{0n}
Δ_{11}	Δ_{12}	. . .	Δ_{1l}	. . .	Δ_{1n}
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
Δ_{k1}	Δ_{k2}	. . .	Δ_{kl}	. . .	Δ_{kn}

D

Fig.1

Table B is composed of precalculated values of b_{pq}. In the first line of Table D the components of the approximation x_0 are entered. This Table is further filled out with successive lines beginning with the line

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containing the changes Δ_{oj}. The values of Δ_{oj} are determined according to eq.(6) and the residues r_{oi} $(i = 1, 2, \ldots, n)$ are obtained by putting the vectors x_o in the system (1). For filling up the remaining line eq.(8) is then used. The content of one line corresponds to one iterative step. The "executed" changes in each of the steps are underlined in Table D. The values of $b_{jl} = b_{lj}$ required for the calculation of $\Delta_{k+1,j}$ for all $j = 1, 2, \ldots, n$ according to eq.(8) form the lth line of Table B.

In operating according to this improved method, we do not calculate the residues r_{ki} at the individual steps. Since eq.(5) is valid, it is sufficient to calculate $\sum_{i=1}^{n} r^2_{k+1,i}$ (the residue r_{oi} was determined before the calculation of Δ_{oj}), and further the expression $\sum_{i=1}^{n} r^2_{k+1,i}$, after which we can determine according to eq.(5) in succession for $k = 0, 1, 2, \ldots$

Also with this method (in view of the rounding of errors) it is advisable occasionally to calculate the last approximation of the component to be put in the system (1) and then to proceed with the iterative process in starting with this "corrected" residue.

4. Remarks. It can be shown that the method of minimization of the sum of the squares of the residues applied to the system $Ax - a = 0$ corresponds to the Gauss-Seidel method applied to the system $A'Ax - A'a = 0$. While at the Gauss-Seidel iterative process, the component x_{kj} is changed in succession in the order of the index j, with the method of minimization of the sum of the squares of the residues the possibility is utilized of increasing the "efficiency" of the iterative step by corresponding selection of the component to be changed at the given step. Moreover, at calculation according to the Gauss-Seidel method the whole iterative process is usually carried out directly with the approximate values of the components, while with the method of minimisation of the squares of the residues, the iterative process is carried out only on the increments Δ. This method is alr-

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very closely connected with the Southwell relaxation method.

The described method is applicable to any system of linear algebraic equations (with non-zero determinants), and can be advantageously used for calculations on the automatic computer. For the solution of systems of linear equations on this machine, it is necessary with most of the previous methods to store in the machine the whole matrix A of the system, which occupies n^2 memories of the machine. The calculation according to the method described in this article can be planned in such a way that it is sufficient to store in the machine of the elements of matrix A only those elements which lie above the diagonal in Table B, which occupy only $\frac{n(n-1)}{2}$ memories. From this it follows that with this method it will be possible to solve on the automatic computer, systems with a larger number of equations than is possible with the previous methods.

SUMMARY

The article proposes a new iterative method for the solution of a system of linear algebraic equations. The method was worked out in the course of work on a universal method of solving systems of linear equations suitable for an automatic computer. The original method, as presented by A.Svoboda at the Discussion Afternoons on Machines for Processing Information, is described in Par.2. The proposed new procedure, which fundamentally reduces the number of operations performed at each iteration, is described in Par.3. It is prepared in such a way that it is also possible to use it easily on normal calculating machines, and a simple computation table is proposed.

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INTERPOLATION ON BASIS OF VALUE OF FUNCTION INSIDE INTERPOLATION INTERVAL*

by

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Introduction

Toward the end of 1953 the national enterprise Aritma brought onto the market the first "calculation perforator" produced in series according to the project of

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* Presented to the Second Regular All-State Conference of the Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences in December 1953.

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Docent Dr. A. Svoboda: The calculation perforator supplements the line of machines for processing perforated cards of Czechoslovakian production, and is a very important contribution to the apparatuses capable of carrying out the four fundamental arithmetical operations, and also with respect to the sign. At the laboratory investigation of the prototype of the calculation perforator it was found that it not only satisfies all of the requirements for a machine for processing perforated cards of statistics and accounting, but that with it many problems of a mathematical nature can also be solved.

The calculation perforator is advantageously applicable especially to parallel (mass) calculations, as, for example, the evaluation of formulas containing a large number of different values of individual independent variables. The operational speed of the machine is considerable. The machine carries out, for example, 6000 multiplications per hour or compoundings of two seven-place numbers*, or 3000 divisions. In one operation the card is scanned, the calculation operation carried out, and the result perforated in the same or the next card. The registration of intermediate results, their restorage in the machine is wholly eliminated from the calculation, thereby dispensing, for example, with the necessity of a computer Table. Through this the operating speed of the calculation perforator is increased still further, and at the same time the possibility of errors due to the human factor is practically limited to the preparatory part of the calculation, i.e., to the perforation of the calculation values in the cards. (For further details on the calculation perforator and the operations with perforated cards, see Collection I of works in the field of machines for processing information [Bibl.1].)

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* At the execution of numerical calculation the full capacity of the calculation perforator is usually not utilized, which can, for example, multiply 12-place by seven-place numbers and perforate the results to 12 places, or compound two 11-place numbers.

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For the solution of certain problems, it is necessary to introduce into the calculation the values of functions whose calculation is fairly tedious (goniometrical functions, elliptical integrals, etc) or which are obtained experimentally. In this case it is more advantageous to calculate the corresponding functional values from Tables with the help of the corresponding interpolation formulas. The Tables of the functional values with the corresponding arguments and interpolation coefficients are perforated once for always in the cards, which are provided with the mark of the main card. In this way each "tabular" card contains all of the information for the interpolation in the interval between the argument on the same card and the argument on the next tabular card. When linear interpolation is sufficient each tabular card contains the value of the tabular argument x_k, the corresponding value of the function $f(x_k) = f_k$, and the first difference $\Delta_k = f_{k+1} - f_k$, $(k = 1, 2, \ldots)$. The step, i.e., the difference between two successive tabular arguments, $h = x_{k+1} - x_k$ is a whole power of 10. In the "calculation card"* the argument $x = x_{k+n}$ is perforated (usually in the form of the result of the preceding operation). The functional value corresponding to this argument is calculated according to the formula

$$f_{k+n} = f_k + \Delta_k n, \quad (0 \leq n < 1).$$

The value $n = (x_{k+n} - x_k)/h$ is taken by the machine directly from the card field of the argument x_{k+n} only at those decimal places whose order is smaller than the order of step h. The interpolation is carried out in such a way that the pack of tabular cards according to the argument is arranged in the sorter relative to the pack of calculation cards, after which we carry out on the calculation perforator the operations "multiplication and compounding of the main card and the next card". The value Δ_k is taken by the calculation perforator from the kth tabular

* That is, the card on which the given problem is solved.

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(main) card and retained in the memory until the arrival of the next tabular card. From each of the calculation cards following the tabular card the machine takes the value n, multiplies it by the value Δ_k stored in the memory, and perforates the result in the same card. At the second transit of the pack through the calculation perforator the machine takes from the tabular card the value f_k and adds it to the value perforated in the calculation card at the preceding transit of the pack. The sum is again perforated in the same card. This completes the linear interpolation, and for each argument contained on the calculation card, the corresponding value of the function is also perforated.

It is known (Bibl.2) that for the absolute value of the interpolation error of a linear interpolation, the following is valid

$$|\varepsilon_i| \leq \tfrac{1}{8}h^2 f''(\xi), \quad (x_i < \xi < x_{i+1}).$$

Therefore, at the required precision of calculation each function has a certain maximal magnitude of step h. Thus, for example, for sine in the range of 0^g to 100^g and for $\varepsilon \leq 0.5 \times 10^{-6}$ there must be maximally

$$h = \sqrt{\frac{8 \cdot 0{,}5 \cdot 10^{-6}}{1}} = 2 \cdot 10^{-3} = 0{,}115^g.$$

For the requirement that h must be a whole power of ten, therefore, the step h $h = 0.1^g$ is satisfied. The Table of sines for the range of 0^g to 100^g, therefore, contains 1000 tabular cards.

If greater precision is required, for example, $\varepsilon \leq 0.5 \times 10^{-7}$, then the step 7 must be decreased ten times*, which means increasing the pack to 10,000 tabular cards. For a thickness of 0.18 mm per card this represents a "pack" 1.80 m thick. The addition of such a number of cards to the pack of calculation cards, which usually contains only a few hundred cards, and the passage of the whole pack

* At mechanical calculation it is economical for h to be a whole power of ten.

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of cards through the calculation perforator would take too much time. Moreover, most of the cards in the pack do not even participate in the calculation. Consequently, it is better to use a small number of tabular values and interpolate to a higher degree. At present the interpolation formulas are used for calculating the functions in certain intervals of the values of the functions of the boundaries and outside these intervals as well as differences of these values. Therefore, we say that according to such formulas we carry out the interpolation on the basis of the information on the functions outside the interpolation interval. If we use the formulas for interpolation on the basis of the information on the functions inside the interpolation interval, we increase considerably the precision of the interpolation at the same range of the Tables, as will be shown below.

1. Interpolation on Basis of Value of Function Outside Interpolation Interval

Usually in the functional Tables the values $f(x_k)$ (hereafter shortened to f_k) of the equidistant arguments x_k ($k = 0, 1, 2, \ldots$) are given, whose steps $h = x_{k+1} - x_k$ are whole powers of ten. Besides the arguments x_k and their corresponding functional values f_k, the difference of the 1st order (1st differences) are given in the Tables

$$\Delta_k = f_{k+1} - f_k, \quad (k = 0, 1, 2, \ldots),$$

the differences of the 2nd order (2nd differences)

$$\Delta_k^2 = \Delta_{k+1} - \Delta_k, \quad (k = 0, 1, 2, \ldots)$$

etc., for cases where the only differences are of even order or so-called average differences.

1.1 Newtonian Interpolation Formula. Most of the formulas for the interpolation of polynomials of the ith degree can be derived from Newton's formula

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$$f(x) = f_k + \frac{x - x_k}{1!}\frac{\Delta_k}{h} + \frac{(x - x_k)(x - x_{k+1})}{2!}\frac{\Delta_k^2}{h^2} + \dots + \frac{(x - x_k)(x - x_{k+1})\dots(x - x_{k+i-1})}{i!}\frac{\Delta_k^i}{h^i} + \varepsilon_i, \quad (1.1)$$

where $f(x) = f(x_{k+n}) = f_{k+n}$ is the value of the function for the argument

$$x = x_{k+n} = x_k + nh, \quad (0 \leq n \leq i, \; h = x_{k+1} - x_k).$$

The remainder (interpolation error) is given by the expression

$$\varepsilon_i = \frac{(x - x_k)(x - x_{k+1})\dots(x - x_{k+i-1})(x - x_{k+i})}{(i+1)!} f^{(i+1)}(\xi), \; (x_k < \xi < x_{k+i}). \quad (1.2)$$

By putting in eqs.(1.1) and (1.2) $x = x_{k+n}$ ($h = x_{k+1} - x_k$; $0 \leq n \leq i$), we get

$$f_{k+n} = f_k + \frac{n}{1!}\Delta_k + \frac{n(n-1)}{2!}\Delta_k^2 + \dots + \frac{n(n-1)(n-2)\dots(n-i+1)}{i!}\Delta_k^i + \varepsilon_i. \quad (1.3)$$

$$\varepsilon_i = \frac{n(n-1)(n-2)\dots(n-i+1)(n-i)}{(i+1)!} h^{i+1} f^{(i+1)}(\xi) \quad (1.4)$$

In the remainder ε_i occurs the function

$$X_i = \frac{n(n-1)(n-2)\dots(n-i+1)(n-i)}{(i+1)!} = \frac{(x - x_k)(x - x_{k+1})\dots(x - x_{k+i-1})(x - x_{k+i})}{(i+1)!\,h^{i+1}}, \quad (1.5)$$

which is a curve of the (i + 1)th degree with zero value for $x = x_k, x_{k+1}, \dots x_{k+i}$, i.e., for $n = 0, 1, 2, \dots, i$. The absolute values of its extremes are usually minimal in the middle part of the whole interval (x_k, x_{k+i}) or $(0,i)$.

In Fig.1 the course of the function X_i for $i = 1, 2, 3, 4, 5$ is represented.

The interpolation is usually carried out only between two tabular arguments, i.e., only in one of the i possible interpolation intervals h. Therefore, for

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$0 < n < 1$ or for $1 < n < 2$, etc. to $i - 1 < n < i$. It is seen that the greatest interpolation error occurs in the first and the last intervals of i possible interpolation intervals.

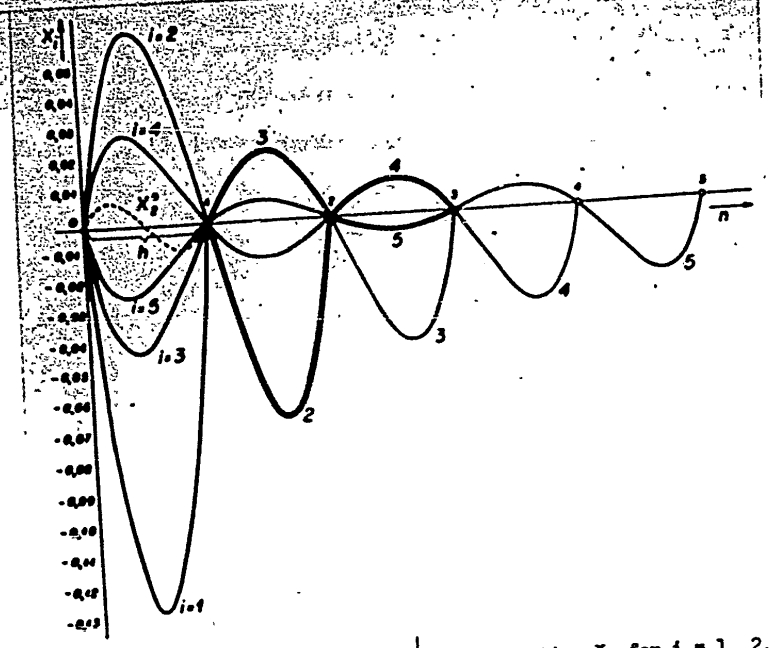

Fig.1 – Graphic Representation of the Function X_i for i = 1, 2, 3, 4, 5. Heavy parts of curve represent parts of function occurring in remainder ε_i of Gauss's interpolation formula

Besides the interpolation error ε_i, the interpolated functional value is burdened with the tabular error ε_t, which is due to the fact that in the interpolation formula not the precise functional values and the precise rounded difference have been put, but the tabular values and the difference from them. The tabular error must, at interpolation of a higher degree, reach a fairly great value (see Fig.2). In the most unfavorable case of resolution of the rounded error of the tabular value,

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the absolute value of the tabular error of the interpolation of the ith degree is

$$|\varepsilon_t| \leq \varepsilon + \varepsilon \sum_{k=1}^{i} (-1)^{k+1} (2^k - 2) \frac{n(n-1)\dots(n-k+1)}{k!}, \qquad (1.6)$$

$$(\varepsilon = 0{,}5e,\ 0 \leq n \leq i),$$

where e denotes the unity of the last valid place.

In Fig.2 the course of the tabular error for the interpolation of the ith degree ($i = 1, 2, 3, 4, 5, 6$) with unfavorable situation of the rounded error of the tabular value is represented.

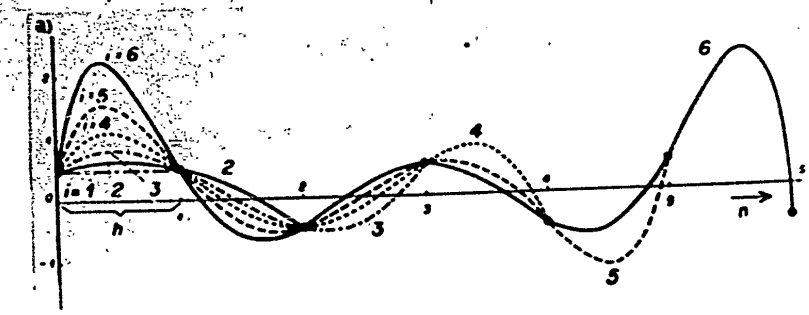

Fig.2 - Course of Tabular Error ε_t (in Unity of Last Valid Place of Interpolation of ith Degree for $i = 1, 2, 3, 4, 5, 6$ at Unfavorable Occurrence of Rounded Error of Tabular Value

a) In unity of last place

In this case, when the division sign of the rounded error of the tabular value is selected in such a way that the maximal tabular error is in the interval (x_k, x_{k+1}) (or expressed for n in the interval [0.1]), it can be seen from Fig.2 that the tabular error (as also the interpolation error) in the interpolation interval of the middle part of the whole interval (x_k, x_{k+1}) (or for n in the interval [0,i]) is much smaller than at the ends of the interpolation interval. Therefore, when possible we use interpolation of the middle interval of (x_k, x_{k+1}) for example, for $i/2 \leq n \leq i/2 + 1$, if it is an even number.

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1.2 Gauss's Interpolation Formula. We arrange Newton's interpolation formula in such a way that for $0 \le n \le 1$ this interpolation is carried out in the middle part of the interval (x_k, x_{k+1}) where the interpolation error is minimal, and when we also express the difference Δ^l_k, $(l = 1, 2, \ldots, i)$ with the help of the average difference, i.e., in such a way that in the Table the differences (see Fig.3) lie on the same or adjacent lines, as is the case with the tabular values f_k obtained with Gauss's interpolation formula for $0 \le n \le 1$, then we have

$$f_{k+n} = f_k + \frac{n}{1!}\Delta_k + \frac{n(n-1)}{2!}\Delta^2_{k-1} + \frac{n(n^2-1)}{3!}\Delta^3_{k-1} + \frac{n(n^2-1)(n-2)}{4!}\Delta^4_{k-2} + \ldots + \varepsilon_i, \quad (1.7)$$

where the interpolation error for even i is

$$\varepsilon_i = \frac{n(n^2-1)(n^2-2^2)\ldots\left(n^2-\left(\frac{i}{2}\right)^2\right)}{(i+1)!} h^{i+1} f^{(i+1)}(\xi), \left(x_{k-\frac{i}{2}} < \xi < x_{k+\frac{i}{2}}\right) \quad (1.8a)$$

and for odd i

$$\varepsilon_i = \frac{n(n^2-1)(n^2-2^2)\ldots\left(n^2-\left(\frac{i-1}{2}\right)^2\right)\left(n-\frac{i+1}{2}\right)}{(i+1)!} h^{i+1} f^{(i+1)}(\xi), \quad (1.8b)$$

$$\left(x_{k-\frac{i-1}{2}} < \xi < x_{k+\frac{(i+1)}{2}}\right).$$

The fraction on the right side of the equations (1.8a) and (1.8b) is identical with the function X_i (1.5) which occurs in the remainder of Newton's interpolation equation for $\frac{i}{2} \le n \le \frac{i}{2} + 1$ if i is even or for $\frac{i-1}{2} \le n \le \frac{i-1}{2} + 1$ if i is odd. In Fig.1 this segment of the function X_i for i = 2, 3, 4, 5 is shown in a heavy line.

The tabular error in the interpolation interval (x_k, x_{k+1}) is therefore maximal at such an extent of the rounded error that the signs of the tabular errors of the values f_k and f_{k+1} are in agreement with each other and the signs of the errors of

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the remaining values alternate their orientations in both directions from f_k and f_{k+1}. The tabular error reaches its extrema value in the middle of the interpolation interval (for $n = 0.5$). Its absolute value may reach at interpolations of the 2nd and 3rd orders the magnitude of 0.625 for the unit of the last place, at interpolations of the 4th and 5th orders the magnitude of 0.696, and for interpolations of the 6th and 7th orders the magnitude of 0.745.

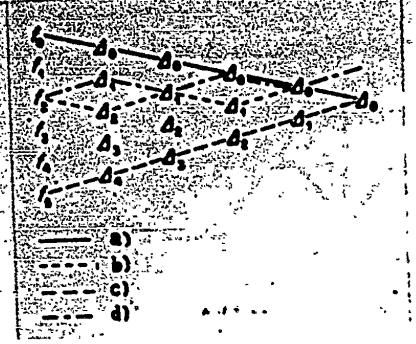

Fig.3 - Tabular Differences; Lines Join Values Occurring in Corresponding Formulas

a) Newton's interpolation forward;

b) Gauss's interpolation forward;

c) Newton's interpolation backward;

d) Gauss's interpolation backward

1.3 Everett's Interpolation Formula.

When in Gauss's equation we replace the difference of odd order with the next lower difference of even order we obtain the the following arrangement of Everett's equation

$$f_{k+n} = mf_k + \binom{m}{3}^{1} \Delta^2_{k-1} + \binom{m}{5}^{2} \Delta^4_{k-2} + \cdots + nf_{k+1} + \binom{n}{3}^{1} \Delta^2_k + \binom{n}{5}^{2} \Delta^4_{k-1} + \cdots \quad (1.9)$$

The interpolation and tabular errors are the same as with Gauss's formula. The Tables arranged for Everett's interpolations are very suitable for printing because they contain only half as many columns as the other Tables for interpolations of the same orders.

According to the above formula we proceed at the interpolation from the fundamental functional value of the argument x_k to the interpolated functional value of the higher argument x_{k+n} (forward interpolation). At backward interpolation we arrange the formula in such a way that we proceed from the fundamental functional

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value of the higher argument x_k to the interpolated functional value of the lower argument x_{k-n}.

1.4 Sterling's Interpolation Formula. By forming the arithmetical average of Gauss's equation for forward interpolation and of Gauss's equation for backward interpolation we obtain Sterling's equation.

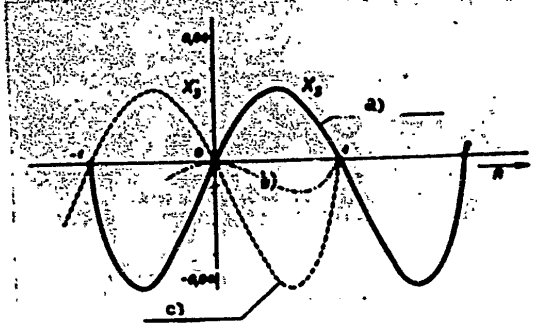

Fig.4 - Function $\frac{X_i + X_i'}{2}$ of Interpolation Error of Sterling's Formula

a) Gauss forward; b) Sterling; c) Gauss backward

Sterling's equation of even order is identical with Gauss's equation of the same order, and both have the same interpolation and tabular errors.

However, the equation of odd order has a considerably smaller interpolation error (especially for $-\frac{1}{2} < n < \frac{1}{2}$) than Gauss's equation, but on the other hand, a somewhat greater tabular error.

Sterling's equation is known:

$$f_{k+n} = f_k + \frac{n}{1!}\frac{(\Delta_{k-1} + \Delta_k)}{2} + \frac{n^2}{2!}\Delta^2_{k-1} + \frac{n(n^2-1)}{3!}\frac{(\Delta^3_{k-2} + \Delta^3_{k-1})}{2} + \ldots + \varepsilon_i . \quad (1.10)$$

1.5 Bessel's Interpolation Formula. By forming the arithmetical average of Gauss's equation for forward interpolation and of Gauss's formula for backward

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interpolation by one step of movement we obtain Bessel's equation.

The formula of even order has the same tabular error as Gauss's formula; the interpolation error, however, is much smaller, especially for n close to $\frac{1}{2}$. Consequently, Bessel's formula can be advantageously employed for the thickening of Tables, i.e., for the calculation of Tables of the step h/2 from the Tables of the step h.

Bessel's equation has the form of

$$f_{k+n} = f_k + \frac{n}{1!}\Delta_k + \frac{n(n-1)}{2!}\frac{(\Delta^2_{k-1} + \Delta^2_k)}{2} + \frac{n(n-1)(n-\frac{1}{2})}{3!}\Delta^3_{k-1} + \ldots + \varepsilon_i. \qquad (1.11)$$

The smaller interpolation error in both of these formulas is due to the fact that at the formation of the arithmetical average of the two Gauss formulas there is also formed the arithmetical average of the two mutually-displaced functions X_i which occur in the equation for the interpolation error (see Figs.4 and 5).

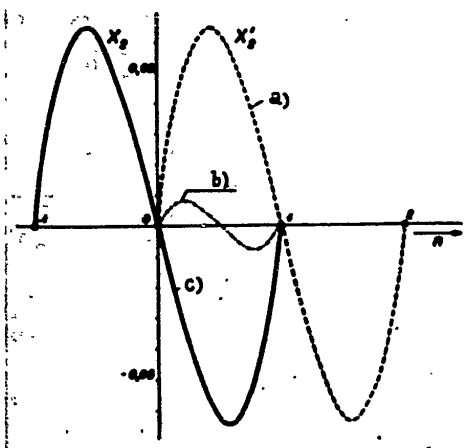

Fig.5 - Function $\frac{X_i + X_i'}{2}$ of Interpolation Error of Bessel's Formula of 2nd Order.

a) Gauss (moving) backward; b) Bessel; c) Gauss forward

2. Interpolation on Basis of Value of Function Inside Interpolation Interval

When we examine the suitability of these formulas for application to interpolation with perforated-card machines, we find that none of them is suitable in the original form. Thus, for example, Everett's equation is employed for interpolation of two nei-

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boring tabular values and their corresponding average even difference. These values must be perforated in individual cards, so that the savings obtained at the printing of the Tables for the Everett interpolations are not reflected in a small number of tabular cards and perforated values. In this respect Everett's formula differs from Gauss's formula. The main disadvantage with all of the formulas is that for each n it is necessary before carrying out the interpolation to find a different "binomial" coefficient. At manual calculation the work is facilitated by the fact that these coefficients are found in the Tables. At calculation on the calculation perforator, however, the tabulation cards which are added to the pack of calculation cards are inaccessible, and direct calculation of the coefficients is too complicated. With any interpolation formula, therefore, it is necessary to arrange in advance to distinguish between the products of the multiplications, and after compounding the individual terms to arrange them in descending powers of n. In this way, the interpolation coefficients are obtained for the powers of n which are the linear combinations of the differences entered in the Tables. Since for machine purposes we must calculate these new interpolation coefficients anyway, we use for their calculation not the information on functions outside the interpolation interval (i.e., for example, the functional values f_{k-2}, f_{k-1}, f_k, f_{k+1}, f_{k+2}, f_{k+3} in the formula of the 5th order) but the information on functions inside the interpolation interval (i.e., for example, the value of f_k, $f_{k+0.2}$, $f_{k+0.4}$, $f_{k+0.6}$, $f_{k+0.8}$, f_{k+1}), by which we reach a much better approximation*.

2.1 Interpolation on Basis of Value of Function Inside Interpolation Interval.

Divide each interpolation interval (x_k, x_{k+1}), $(k = 0, 1, 2, \ldots)$ into i equidistant subintervals

* A method for the interpolation of one variable for division of the interpolation interval into i equidistant subintervals and its employment especially for extending calculating machines for the calculation of functional Tables was published in 1951 by K.Ramsay (Bibl.3).

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$$[x_{k+\frac{l}{i}}, x_{k+\frac{l+1}{i}}] = h^*, \ (k = 0, 1, \ldots; \ l = 0, 1, \ldots, i-1).$$

We assume further that there are known in all of the end points x_k, $x_{k+1/i}$, ..., x_{k+1} of the subintervals, i.e., at the boundaries and inside the interpolation intervals, the corresponding functional values f_k, $f_{k+1/i}$, ..., $f_{k+i/i}$.

The individual subintervals may therefore be regarded as new interpolation intervals with the steps of the argument $h^* = \frac{h}{i}$ divided in such a way that the interpolation is carried out over all i subintervals. The difference of the corresponding steps "h" is denoted by a dash. In this case, according to eq.(1.1) Newton's interpolation formula is

$$f(x) = f_k + \frac{x - x_k}{1!}\frac{\bar{\Delta}_k}{h^*} + \frac{(x - x_k)(x - x_{k+\frac{1}{i}})}{2!}\frac{\bar{\Delta}_k^2}{h^{*2}} + \ldots + \frac{(x - x_k)(x - x_{k+\frac{1}{i}})\ldots(x - x_{k+\frac{i-1}{i}})}{i!}\frac{\bar{\Delta}_k^i}{h^{*i}} + r_i^* \qquad (2.1)$$

where the remainder is

$$r_i^* = \frac{(x - x_k)(x - x_{k+\frac{1}{i}})\ldots(x - x_{k+\frac{i}{i}})}{(i+1)!} f^{(i+1)}(\xi), \ (x_k < \xi^* < x_{k+1}). \qquad (2.2)$$

For $x_k \leq x \leq x_{k+1}$ and for $0 \leq n \leq 1$ the following relations are valid:

$$x = x_{k+n} = x_k + nih^*, \ \text{if} \ h^* = x_{k+\frac{l+1}{i}} - x_{k+\frac{l}{i}}, \ (l = 0, 1, \ldots, i-1). \qquad (2.3)$$

$$x_{k+\frac{l}{i}} = x_k + lh^*, \ (l = 0, 1, \ldots, i). \qquad (2.4)$$

By putting eqs.(2.3) and (2.4) in eq.(2.1) we get the formula for interpolation on the basis of the interval values

$$f(x) = f_{k+n} = f_k + \frac{n}{1!}i\bar{\Delta}_k + \frac{n\left(n - \frac{1}{i}\right)}{2!}i^2\bar{\Delta}_k^2 + \ldots + \qquad (2.5)$$

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$$\frac{n\left(n-\frac{1}{i}\right)\left(n-\frac{2}{i}\right)\cdots\left(n-\frac{i-1}{i}\right)}{i!}\,i^{i}\bar{\Delta}_k^i + \varepsilon_i^*. \tag{2.5}$$

where

$$\bar{\Delta}_k = f_{k+\frac{1}{i}} - f_k,\ \bar{\Delta}_{k+\frac{1}{i}} = f_{k+\frac{2}{i}} - f_{k+\frac{1}{i}},\ \ldots,\ \bar{\Delta}_k^2 = \bar{\Delta}_{k+\frac{1}{i}} - \bar{\Delta}_k,\ \ldots,\ \bar{\Delta}_k^i = \bar{\Delta}_{k+\frac{i-1}{i}}^{i-1} - \bar{\Delta}_k^{i-1}.$$

By putting eqs.(2.3) and (2.4) in eq.(2.2) we get the expression for the interpolation error

$$\varepsilon_i^* = \frac{n\left(n-\frac{1}{i}\right)\left(n-\frac{2}{i}\right)\cdots\left(n-\frac{i-1}{i}\right)\left(n-\frac{i}{i}\right)}{(i+1)!}\,i^{i+1}h^{*i+1}f^{(i+1)}(\xi^*),$$

$$\text{at}\quad x_k < \xi^* < x_{k+1}. \tag{2.6}$$

If we still get $h^* = \frac{h}{i}$ and write after it n^* instead of n^*)we get

$$\varepsilon_i^* = \frac{n^*\left(n^*-\frac{1}{i}\right)\left(n^*-\frac{2}{i}\right)\cdots\left(n^*-\frac{i}{i}\right)}{(i+1)!}\,h^{i+1}f^{(i+1)}(\xi^*)\ \text{for}\ 0 \leq n^* \leq 1$$

$$\text{and}\ [x_k, x_{k+1}]. \tag{2.7}$$

The fraction on the right side of expression (2.7)

$$X_i^* = \frac{n^*\left(n^*-\frac{1}{i}\right)\left(n^*-\frac{2}{i}\right)\cdots\left(n^*-\frac{i}{i}\right)}{(i+1)!} \tag{2.8}$$

is a function of n^* [curve of the $(i+1)^{th}$ degree] with zero value for $n^* = 0, \frac{1}{i}, \frac{2}{i}, \ldots, 1$. In Fig.1 the dotted line represents this function for i=2.

*) For avoiding confusion we use the denotation n^* for distinguishing the interpolation error ε_i from the interpolation error ε_i of the Newtonian formula.

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The extreme value of the function X_i^* is in absolute value i^{i+1} times smaller than the extreme value of the function X_i which occurs in the expression for the interpolation error of Newton's eq.(1.5).

Equation (2.8) is valid for $0 \leq n^* \leq 1$. In order to be able to compare it with the analogous eq.(1.5), which occurs in the expression for the interpolation error of Newton's formula and is valid for $0 \leq n \leq i$, we multiply the numerator and the denominator by the number i^{i+1}.

This gives

$$X_i^* = \frac{in^*(in^* - 1)(in^* - 2)\dots(in^* - i)}{i^{i+1}(i+1)!} \quad \text{for} \quad 0 \leq in^* \leq i.$$

By comparison with eq.(1.5), i.e., with

$$X_i = \frac{n(n-1)(n-2)\dots(n-i)}{(i+1)!} \quad \text{for} \quad 0 \leq n \leq i$$

we see that

$$X_i^* = \frac{X_i}{i^{i+1}}$$

On the assumption that $f^{(1+i)}(\xi) \doteq f^{(i+1)}(\xi^*)$, where $x_k < \xi < x_{k+i}$; $x_k < \xi^* < x_{k+1}$, therefore, the error is

$$\varepsilon_i^* \doteq \frac{\varepsilon_i}{i^{i+1}},$$

which is obvious since any of the steps in Newton's interpolation formula is i times smaller. Thus, for example, the interpolation error of Newton's formula of the 2nd order is

$$\varepsilon_i = \frac{n(n-1)(n-2)}{6} h^3 f'''(\xi) \tag{2.9}$$

and for $n_1 = 0.423$ and $n_2 \doteq 1.577$ we have

$$|\varepsilon_i|_{max} \doteq 0{,}064\, h^3 f'''(\xi), \ (x_k < \xi < x_{k+2}).$$

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Therefore, the error of the interpolation formula of the same order on the basis of the interval value according to eq.(2.7)

$$\varepsilon_i^* = \frac{n^*(n^* - \frac{1}{2})(n^* - 1)}{6} h^3 f'''(\xi^*), \ (0 \leq n^* \leq 1),$$

has for $N_1^* \doteq 0.2113$ and $n_2^* \doteq 0.7887$

$$|\varepsilon_i|_{max} \doteq 0{,}008 h^3 f'''(\xi^*), \ (x_k < \xi^* < x_{k+1}).$$

At interpolation according to both formulas it is necessary to calculate the same values. For Newton's equation f_k, Δ_k, Δ_k^2; for the other equation f_k, Δ_k, Δ_k^2, where

$$\Delta_k = f_{k+1} - f_k, \ \Delta_k^2 = \Delta_{k+1} - \Delta_k, \ (\Delta_{k+1} = f_{k+2} - f_{k+1}),$$

and

$$\bar{\Delta}_k = f_{k+1} - f_k, \ \bar{\Delta}_k^2 = \bar{\Delta}_{k+1} - \bar{\Delta}_k, \ (\bar{\Delta}_{k+1} = f_{k+1} - f_{k+1}).$$

The interpolation error of Bessel's formula is nearly the same as the error of the formula based on the internal values. For Bessel's formula, however, it is necessary to know not only f_k and Δ_k but also the values of $\frac{\Delta_{k+1}^2 + \Delta_k^2}{2}$ which are not tabulated.

In Fig.6 the Table of the extreme values of the function X_i and the function X_i^* for the interpolations of the first to the fifth degree is presented.

The degrees i of the polynominal are in the first column. In the second column are listed the values of n, $(0 < n < i)$ for which the extreme values of the function X_i are obtained at the Newtonian interpolation. These extreme values are listed in the third column. In the fourth column are listed the values of N^* $(0 < n^* < 1)$ for which the extreme values of the function X^* are obtained at interpolation on the basis of the formation on the function inside the interpolation interval (x_k, x_{k+1}). Finally, in the fifth column are listed the corresponding ex-

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trema values.

The values printed in bold-faced type in the third column are the extreme values occurring at the employment of, for example, Gauss's and Everett's formulas

i	n $(0 \leq n \leq 1)$	$x_i = \frac{n(n-1)\ldots(n-i)}{(i+1)!}$	n^* $(0 \leq n^* \leq 1)$	$x_i^* = \frac{n(n-1)\ldots(n-1)}{(i+1)!}$
1	0,500	−0,125	0,5	−0,125
2	0,423	+0,064	0,21	+0,008
	1,577	−0,064	0,79	−0,008
3	0,382	−0,04	0,127	−0,000 5
	1,500	+0,023	0,500	+0,000 3
	2,618	−0,04	0,873	−0,000 5
4	0,356	+0,03	0,089	+0,000 03
	1,456	−0,012	0,364	−0,000 012
	2,544	+0,012	0,635	+0,000 012
	3,644	−0,03	0,911	−0,000 03
5	0,337	−0,023	0,067	−0,000 001 5
	1,426	+0,007	0,285	+0,000 000 5
	2,500	−0,005	0,500	−0,000 000 3
	3,574	+0,007	0,715	+0,000 000 5
	4,663	−0,023	0,933	−0,000 001 5

Fig.6 - Extreme Values of Functions x_i and x_i^* Occurring in Formulas for Interpolation Errors ε_i and ε_i^*

(see also heavy-line curve in Fig.1). In the fifth column the minimal or maximal extreme values which the function X_i^* can reach in the interpolation interval (x_k, x_{k+1}) are underscored. By comparing these bold-faced values with each other an idea can be obtained of the height of the precision at the employment of the formulas of the same order for interpolation on the basis of the interval values or the possibility of lowering the order of the interpolation with retention of approximately the same precision. It is clear that for judging the suitability of these interpolations, the second factor $h^{i+1} f^{(i+1)}(\xi) \approx \Delta^{+1}$ of the equation for the interpolation error must also be taken into account, which may be for our interpolations more suitable for some functions and less suitable for others.

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2.2 Interpolation Formula of 2nd Degree. Putting $i = 2$ in eq.(2.5) gives

$$f(x) = f_{k+n} = f_k + n\Delta_k + \frac{n(n-1)}{2}\Delta_k^2 + \varepsilon_i, \qquad (2.11)$$

at which

$$\varepsilon_i = \frac{n(n-1)(n-2)}{3}h^3 f'''(\xi), \text{ where } h = x_{k+1} - x_k \text{ and } \Delta_k = f_{k+1} - f_k \text{ etc.}$$

Equation (2.11) is arranged in the following final form:

$$f_{k+n} = (a_k n + b_k)n + f_k + \varepsilon_i, \text{ where } a_k = 2\Delta_k^2, b_k = 2\Delta_k - \Delta_k^2, 0 \leq n \leq 1. \qquad (2.12)$$

Finally, in the Table we enter for each of the arguments x_k the corresponding functional value of f_k and interpolation coefficients a_k, b_k.

To each of the tabulated arguments, as also for linear interpolation, one perforated card corresponds, in which are perforated, according to the value of the argument, the corresponding value of the function f_k and of the two interpolation coefficients a_k, b_k.

For interpolation on the calculation perforator the cards containing the values of the arguments whose functional values are to be sought are first combined with the pack of tabular cards in such a way that all of the cards are arranged according to the magnitudes of the arguments. The pack of cards arranged in this way is placed in the feeder of the calculation perforator. After the operation "multiplication with main card" the machine is fed the first tabular card, from which the value of the coefficient a_o is palpated, and the card sent to the discharge magazine. The palpated value remains in the memory until the transit of the next tabular card, when the original value is replaced with the new palpated value a_1, etc. If a calculation card comes between two tabulation cards the machine at the transit of such a card palpates the value n, i.e., the value by which the value of its argument x_{k+n} exceeds the value of the argument x_k of the preceding tabulation card. The machine-

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multiplies the value n by the value of the coefficient a_k remaining in the memory from the preceding tabulation card, and perforates the result in the card passing through at the time. After transit of the whole pack of cards, therefore, we have on all of the calculation perforation cards besides the argument x_{k+n} also the value of the product a_{kn}. Next, the operation "compounding with main card" occurs on the machine. The pack of cards is again placed in the machine. At the transit of the tabulation card the machine remembers the value of the coefficient b_k, which it adds to the value $a_k n$ present on the tabulation card, and perforates the result $a_k n + b_k$ in the corresponding card. For the next operation "multiplication on same card", the multiplication $(a_k n + b_k) \times n$ is carried out and the perforation of the result. At this last operation the tabulation card also passes through the machine but does not participate in the operation. The operation "compounding with the main card" is repeated at which the functional value f_k is added to the main card, and the interpolation is finished.

By way of example we present a case which although scarcely occurring in practice nevertheless well demonstrates the advantages of this interpolation method.

Assume that we have in a row (say 800) parallel calculations with perforated cards with transfer of the results to their logarithm based on 10. Assume further that a precision of five decimal places is sufficient. The five-place Table contains the logarithms for 9000 four-place arguments. By calculation with the logarithm of the five-place argument the linear interpolation is carried out. This Table perforated in cards would make a "pack" of tabulation cards more than $1\frac{1}{2}$ m thick. With all of these cards 800 calculation cards would have to be combined with the perforated arguments, with which by linear interpolation the corresponding arguments would be calculated.

By carrying out the interpolation on the basis of the interval value of the 2nd order the number of tabulation arguments and hence also of the tabulation cards is lowered to 90 (ninety), which can easily be combined according to the first two

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decimal places with the 800 calculation cards.

Below the part of the Table of log N for the interpolation of the 2nd order is presented. In one tabulation card the values present in one row are perforated. The underscored values are used in the example.

Table of Log N

k	$x_k = N$	$f_k = \log N$	b_k	a_k
0	10 000	00 000	4 337	— 198
1	11 000	04 139	3 945	— 166
2	12 000	07 918	3 616	— 140
3	13 000	11 394	3 337	— 118
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
89	99 000	99 564	. ...	...

$$\log 12\,489 = (-140 \times 0{,}489 + 3\,616) \times 0{,}489 + 07\,918 = 09\,653$$

$$n = 0{,}489 \qquad (a_2 \times n + b_2) \times n + \log N$$

2.3 Interpolation Equation of 3rd Degree. Putting i = 3 in eq.(2.5) gives

$$f(x) = f_{k+n} = f_k + \frac{n}{1}\,3\bar{\Delta}_k + \frac{n(n-\frac{1}{3})}{2}\,9\bar{\Delta}_k^2 + \frac{n(n-\frac{1}{3})(n-\frac{2}{3})}{6}\,27\bar{\Delta}_k^3 + \varepsilon_i \qquad (2.13)$$

at which

$$\varepsilon_i = \frac{n(n-\frac{1}{3})(n-\frac{2}{3})(n-1)}{24}\,h^4 f^{(4)}(\xi),$$

$$\text{where } h = x_{k+1} - x_k,\ \bar{\Delta}_k = f_{k+\frac{1}{3}} - f_k,$$

$$\bar{\Delta}_k^2 = \bar{\Delta}_{k+\frac{1}{3}} - \bar{\Delta}_k,\ (\bar{\Delta}_{k+\frac{1}{3}} = f_{k+\frac{2}{3}} - f_{k+\frac{1}{3}}),\ \bar{\Delta}_k^3 = \bar{\Delta}_{k+\frac{1}{3}}^2 - \bar{\Delta}_k^2.$$

This formula is again arranged in the final form of

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$$f_{k+n} = ((a_k n + b_k) n + c_k) n + f_k + \varepsilon_1, \tag{2.14}$$

where

$$a_k = \tfrac{9}{2}\bar{\Delta}_k^2 \tag{2.15}$$

$$b_k = \tfrac{9}{2}\bar{\Delta}_k^2 - \tfrac{9}{2}\bar{\Delta}_k^2 \tag{2.16}$$

$$c_k = 3\bar{\Delta}_k - \tfrac{3}{2}\bar{\Delta}_k^2 + \bar{\Delta}_k^2. \tag{2.17}$$

For the composition of the Table and the calculation of the corresponding interpolation coefficients we use as much as possible existing Tables with fewer steps giving the functional values of the arguments with a larger number of decimal places than necessary.

This Table, however, does not contain the functional values of the arguments $x_{k+1/3}$ and $x_{k+2/3}$. Therefore it is more advantageous for the calculation of the interpolation coefficients to use the functional values of the arguments a_k, $a_{k+0.3}$, $x_{k+0.7}$, x_{k+1}. Then the interpolation coefficients are

$$a_k = \tfrac{1}{21}(100\Delta_k - 250\bar{\Delta}_{k+0.3}). \tag{2.18}$$

$$b_k = \tfrac{1}{21}(-100\Delta_k - 100\bar{\Delta}_k + 325\bar{\Delta}_{k+0.3}). \tag{2.19}$$

$$c_k = \Delta_k - a_k - b_k, \tag{2.20}$$

where $\Delta_k = f_{k+1} - f_k$, $\bar{\Delta}_k = f_{k+0.3} - f_k$, $\bar{\Delta}_{k+0.3} = f_{k+0.7} - f_{k+0.3}$.

The corresponding interpolation error is given by the expression

$$\varepsilon_3 = \frac{n(n-0{,}3)(n-0{,}7)(n-1)}{24} h^4 f^{(4)}(\xi), (h = x_{k+1} - x_k, x_k < \xi < x_{k+1}). \tag{2.21}$$

The polynomials of the 3rd degree with these coefficients are very close to the Cebysev polynomials of the 3rd degree, which acquire for the arguments

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$x_{k+0.000}$, $x_{k+0.300}$, $x_{k+0.601}$, $x_{k+0.903}$

the same values as the interpolation functions. The extreme values of the functions occurring in the equation for the remainder ε_3 are therefore in absolute value close to the same magnitude in all three subintervals. Figure 7 graphically represents the function X_3 (i.e., the factor $h^4 f^{(4)}[\xi]$ in the expression for the interpolation error) both for division of the interpolation interval (x_k, x_{k+1}) into three equidistant subintervals and for division into three subintervals with extreme values

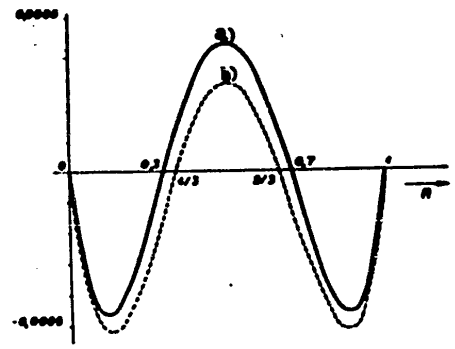

Fig.7 - Function of Formula for Interpolation Error

$$\varepsilon_i = X_3 h^4 f^{(4)}(\xi)$$

a) Division of interpolation interval at points $x_{k+0.3}$, $x_{k+0.7}$; b) Division of interpolation at points $x_{k+1/3}$, $x_{k+2/3}$

of x_k, $x_{k+0.3}$, $x_{k+0.7}$, x_{k+1}.

2.4 Tabulation Error of Interpolation on Basis of Value of Function Inside Interpolation Interval. The interpolation formula of the second order has the form of

$$f_{k+n} = a_k n^2 + b_k n + f_k, \quad (a_k = 2\bar{\Delta}_k^2, \; b_k = 2\bar{\Delta}_k - \bar{\Delta}_k^2) \qquad (2.22$$

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Instead of the precise functional values f_k, $f_{k+1/2}$, f_{k+1}, we actually have the tabulated rounded values

$$f_k^* = f_k - \varepsilon_k,\ f_{k+\frac{1}{2}}^* = f_{k+\frac{1}{2}} - \varepsilon_{k+\frac{1}{2}},\ f_{k+1}^* = f_{k+1} - \varepsilon_{k+1}$$

and the coefficients a* and b* are calculated from the rounded values f_k^*, $f_{k+1/2}^*$, f_{k+1}^*. The most favorable case, for example, when for

$$|\varepsilon_k| = |\varepsilon_{k+\frac{1}{2}}| = |\varepsilon_{k+1}| = \varepsilon = 0.5e$$

(where e is the last valid place at which rounding is carried out), we have

$$f_k^* = f_k - \varepsilon \qquad \bar{\Delta}_k^* = (f_{k+\frac{1}{2}} - \varepsilon) - (f_k - \varepsilon) = \bar{\Delta}_k$$

$$f_{k+\frac{1}{2}}^* = f_{k+\frac{1}{2}} - \varepsilon \qquad \bar{\Delta}^{*2} = \bar{\Delta}^2 + 2\varepsilon.$$

$$\bar{\Delta}_{k+\frac{1}{2}}^* = (f_{k+1} + \varepsilon) - (f_{k+\frac{1}{2}} - \varepsilon) = \bar{\Delta}_k + 2\varepsilon$$

$$f_{k+1}^* = f_{k+1} + \varepsilon$$

It is clear that

$$a_k^* = 2\bar{\Delta}_k^{*2} = 2\bar{\Delta}_k^2 + 4\varepsilon = a_k + 4\varepsilon$$
$$b_k^* = 2\bar{\Delta}_k^* - \bar{\Delta}_k^{*2} = 2\bar{\Delta}_k - \bar{\Delta}_k^2 - 2\varepsilon = b_k - 2\varepsilon,$$

where the asterisks denote values of small precision. Putting eq.(2.22) in the interpolation gives

$$f_{k+n}^* = a_k^* n^2 + b_k^* n + f_k^* = (a_k + 4\varepsilon) n^2 + (b_k - 2\varepsilon) n + f_k - \varepsilon \qquad (2.23)$$

and comparison with the original eq.(2.22) gives

$$f_{k+n}^* = f_{k+n} + 4\varepsilon n^2 - 2\varepsilon n - \varepsilon = f_{k+n} - \varepsilon_t. \qquad (2.24)$$

In this case, therefore, the errors are

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$$\varepsilon_t = \varepsilon(1 + 2n - 4n^2), \quad (\varepsilon = 0{,}5e).$$

The tabulation error has for n = 0.25 the extreme value $(\varepsilon_t)_{max} = 0.625$ at the unit of the last valid place. It is therefore the same as at interpolation according to Newton's equation of the second order, which is also clear from the formulation for the tabulation error (1.6). According to this formula the tabulation error does not depend on either the magnitude of the step h or on the interpolated function or its derivatives.

2.5 Coefficient Error. The coefficient of the interpolation formula of the second degree is calculated from the sum of the multiples of the first and second differences ($a_k = 2\bar{\Delta}_k^2$, $b_k = 2\bar{\Delta}_k - \bar{\Delta}_k^2$).

Otherwise is the case wth the interpolation formulas of the third and higher degrees. The expression according to which the interpolation coefficient is calculated contains only the sum of the multiples of the differences. The calculated coefficient therefore has a larger number of decimal places than the tabulated value of the function. The rounded calculated coefficient is used for the interpolation of the "coefficient error", which is annexed to the tabulated error.

With the interpolation formula of the third degree, a coefficient error occurs both at employment of the coefficient calculated at the equidistant division of the interpolation interval case ($a_k = \frac{9}{2}\bar{\Delta}_k^3$, $b_k = \frac{9}{2}\bar{\Delta}_k^2 - \frac{9}{2}\bar{\Delta}_k^3$, $c_k = 3\bar{\Delta}_k - \frac{3}{2}\bar{\Delta}_k^2 + \bar{\Delta}_k^3$) and at employment of the coefficient calculated at the division of the interpolation interval close to Cebyser's division [$a_k = (100\Delta_k - 250\bar{\Delta}_{k+0.3})/21$, $b_k = (-100\bar{\Delta}_k - 100\bar{\Delta}_k + 325\Delta_{k+0.3})/21$, $c_k = \Delta_k - a_k - b_k$]. We shall limit ourselves here to investigation of the coefficient error of the formula with the last-mentioned coefficient.

The nonrounded interpolation coefficients calculated from the tabulated functional values of f* according to eqs.(2.18), (2.19), (2.20) are denoted a*, b*, c* (where the asterisk means burdened with a tabulation error). The rounded coefficients

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are denoted $\tilde{a}$, $\tilde{b}$, $\tilde{c}$. We have therefore

$$\tilde{a} + \varepsilon_a = a^*, \quad \tilde{b} + \varepsilon_b = b^*, \quad \tilde{c} + \varepsilon_c = c^*. \tag{2.25}$$

The rounding of the errors $\varepsilon_a, \varepsilon_b, \varepsilon_c$ can be obtained in the unfavorable case of half a unit at the last valid place, at which the rounded coefficients $|\varepsilon_a|$, $|\varepsilon_b|, |\varepsilon_c| \leq |\varepsilon| = 0.5e$ were present (where e denotes the unit of the last valid place). The interpolated value calculated with the help of the nonrounded coefficient is given by the relation

$$f_n^* = ((a^* n + b^*) n + c^*) n + f_0^* \tag{2.26}$$

and the interpolated value calculated with the help of the rounded coefficient by the relation

$$\tilde{f}_n = [[(a^* - \varepsilon_a) n + b^* - \varepsilon_b] n + c^* - \varepsilon_c] n + f_0^* . \tag{2.27}$$

Comparison with eq.(2.26) gives

$$\tilde{f}_n = f_n^* - ((\varepsilon_a n + \varepsilon_b) n + \varepsilon_c) n = f_0^* - \varepsilon_k , \tag{2.28}$$

where ε_k denotes the coefficient error due to burdening through the influence of the rounding of the interpolation coefficient. Therefore

$$\varepsilon_k = ((\varepsilon_a n + \varepsilon_b) n + \varepsilon_c) n . \tag{2.29}$$

It is clear that the coefficient error is the greatest when the rounded errors $\varepsilon_a, \varepsilon_b, \varepsilon_c$ have the same sign. Let us investigate the case where this occurs for $\varepsilon_a > 0, \varepsilon_b > 0$.

If $a^* = \tilde{a} + \varepsilon_a$, $b^* = \tilde{b} + \varepsilon_b$, $(0 < \varepsilon_a \leq 0.5e,\ 0 < \varepsilon_b \leq 0.5e)$, then according to eq.(2.20)

$$c^* = \Delta_0^* - a^* - b^* = \Delta_0^* - \tilde{a} - \tilde{b} - (\varepsilon_a + \varepsilon_b) . \tag{2.30}$$

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If it is valid according to eq.(2.20) also for $\varepsilon_a + \varepsilon_b \leq 0.5e$ that

$$\bar{c} = \bar{a} + \bar{b},$$

then we get by comparison of eq.(2.30) with eq.(2.25) the relation

$$\bar{c} = \bar{c} - (\varepsilon_a + \varepsilon_b) = \bar{c} + \varepsilon_c.$$

If $\varepsilon_a > 0$, $\varepsilon_b > 0$ and $\varepsilon_a + \varepsilon_b \leq 0.5e$, then obviously

$$\varepsilon_c = -(\varepsilon_a + \varepsilon_b) < 0. \tag{2.31}$$

This, however, is clearly not the case when the coefficient of error (2.29) acquires the maximal absolute value.

If $\varepsilon_a > 0$, $\varepsilon_b > 0$ and $\varepsilon_a + \varepsilon_b \geq 0.5e$, then

$$\varepsilon_c = 1 - (\varepsilon_a + \varepsilon_b) > 0, \tag{2.32}$$

because the direction of the rounding is the opposite of the case where $\varepsilon_a + \varepsilon_b \geq 0.5e$. Putting in eq.(2.29) ε_c from eq.(2.32) gives

$$\varepsilon_k = [(\varepsilon_a n + \varepsilon_b) n + 1 - (\varepsilon_a + \varepsilon_b)] n. \tag{2.33}$$

For n = 1 and any ε_a, ε_b which satisfies the condition $\varepsilon_a + \varepsilon_b \geq 0.5e$, it is valid

$$\varepsilon_k = 1.$$

It is clear that for $n < 1$, ε_k reaches its maximal value when $1 - (\varepsilon_a + \varepsilon_b)$ is maximal, i.e., when the following is valid

$$\varepsilon_a + \varepsilon_b \doteq 0{,}5e, \ (0 < \varepsilon_a \leq 0{,}5e, \ 0 < \varepsilon_b \leq 0{,}5e)$$

and when $(\varepsilon_a n + \varepsilon_b)n$ has its maximal positive value. Finally, this expression obviously has for $0 < n < 1$ its maximal positive value for $\varepsilon_a = 0$, $\varepsilon_b = 0.5e$. There-

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fore, according to eq.(2.33) the following is valid

$$\varepsilon_k = (0{,}5en + 0{,}5e)\,n = 0{,}5e(n+1)\,n.$$

ε_k as a variable function of n reaches its extreme value $(\varepsilon_k)_{min} = -0.125e$ for $n = -0.5$, which is outside the interpolation interval. For $0 \le n \le 1$ this function increases monotonously and for $n = 1$ it acquires the value $\varepsilon_k = e$ (where e denotes the unit of the last place) (see Fig.8).

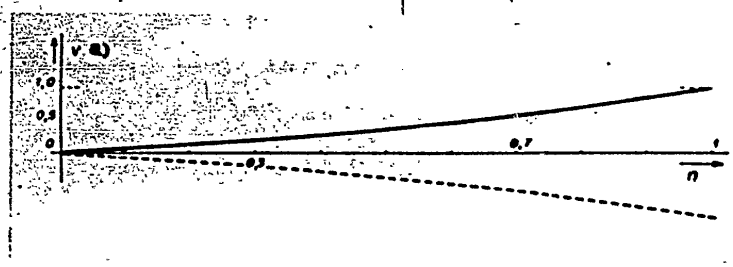

Fig.8 - Graphic Representation of Course of Upper and Lower Limits of Coefficient Error (Coefficients a, b, c Calculated Precisely and Then Rounded)

a) In unit of last place

If, however, we determine the interpolation coefficients in such a way that we first calculate the nonrounded values a*, b* and then round them to values $\bar{a}$, $\bar{b}$ and only then calculate from these rounded values $\bar{c} = \Delta_0^* - \bar{a} - \bar{b}$, then, provided that

$$\bar{a} + \varepsilon_a = a^*, \quad \bar{b} + \varepsilon_b = b^*, \quad \bar{c} + \varepsilon_c = c^*,$$

it is valid that

$$\bar{c} = \Delta_0^* - \bar{a} - \bar{b} = \Delta_0^* - a^* - b^* + \varepsilon_a + \varepsilon_b = c^* + \varepsilon_a + \varepsilon_b = c^* - \varepsilon_c .$$

From this it follows that

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$$\varepsilon_c = -(\varepsilon_a + \varepsilon_b). \tag{2.34}$$

Putting $\varepsilon_c = -(\varepsilon_a + \varepsilon_b)$ in eq.(2.29) gives

$$\varepsilon_k = [(\varepsilon_a n + \varepsilon_b) n - (\varepsilon_a + \varepsilon_b)] n. \tag{2.35}$$

Assume that $\varepsilon_a > 0$, $\varepsilon_b > 0$. Then ε_a and ε_b can reach the maximal value of +0.5 unit of the last valid place. For n = 0 and for n = 1 it is valid that ε_k for any ε_a, ε_b. For $0 < n < 1$ $(\varepsilon_a n + \varepsilon_b)n < \varepsilon_a + \varepsilon_b$ is valid. In other words, a negative binomial always prevails over a positive binomial for any n at which $0 < n < 1$. The preponderance is maximal when $\varepsilon_a + \varepsilon_b$ is maximal, which is the case when $\varepsilon_a = +0.5e$, $\varepsilon_b = +0.5e$. Putting this value in eq.(2.35) gives

$$\varepsilon_k = 0{,}5e((n+1)n - 2)n.$$

The coefficient error $\varepsilon_k = 0.5e(n^3 + n^2 - 2n)$ reaches zero value for n = 0 = 1. It reaches its extreme values in the interpolation intervals for n ≐ 0.549 and $(\varepsilon_k)_{min} \doteq -0.316e$.

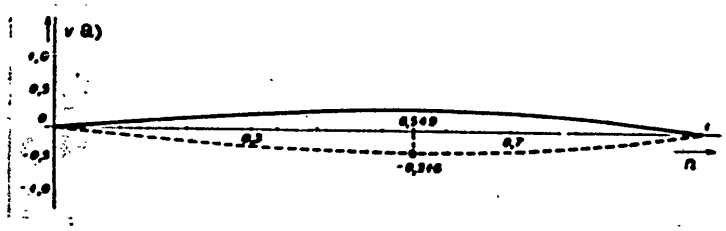

Fig.9 - Graphic Representation of Course of Upper and Lower Limits of Coefficient Error (Coefficient c Calculated and Rounded Coefficients a,b)

a) In unit of last place

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In Fig.9 the course of this "lower limit of the coefficient error" is graphically represented by the dotted line. The solid line represents the course of the upper limit of the coefficient error, i.e., $\varepsilon_a = 0.5e$, $\varepsilon_b = -0.5e$.

It is clear that the interpolation coefficient which is determined by calculating the coefficient c from the rounded values a, b gives at the interpolation a much smaller (by about one third) coefficient error than the coefficient which is first calculated precisely and then rounded.

The coefficient error ε_k is increased or decreased by the tabular error ε_t. Figures 10 and 11 denote by solid lines two cases of an unfavorable course of the tabular error and by dotted lines the course of the upper and lower limits of the coefficient error added to the tabular error. Comparison of the two figures shows that the sum of the tabular error and the coefficient error reaches its extreme value in the case of the course of the tabular error represented in Fig.11 $[(\varepsilon_t + \varepsilon_k)_{min} \doteq 1.003]$. The tabular error itself reaches here the extreme value of $(\varepsilon_t)_{min} \doteq -0.690$, while in the case represented in Fig.10 it reaches the value $(\varepsilon_t)_{max} \doteq +0.726$.

For decreasing the tabular and the coefficient error it is advisable to tabulate the function by one place more precisely than would be done for tabulating the interpolation error, and, after carrying out the calculation, to round the result to the optimal number of places.

3. Interpolation of Function of Two Independent Variables

What has been stated above with respect to the disadvantage of the interpolation methods and the Table of functions of one independent variable for calculation on the calculation perforator applies with even greater force in the case of functions of two independent variables (for example, elliptical integrals or functions of complex variables). Tables of the functions of two independent variables are very voluminous, and the calculation of the interpolated values requires a very large number of operations. For the purposes of the calculation perforator it is unavoidably neces-

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sary to arrange the function Table in such a way that for the suitably-selective fundamental-functional value the corresponding interpolation coefficients are calculated once for always with the help of the functional values present inside the individual parts of the interpolation interval. These interval functional values are

Fig.10 - Unfavorable Course of Tabular Error (Solid Line) and Superposed with Coefficient Error (Dotted Lines)

a) In unit of last place

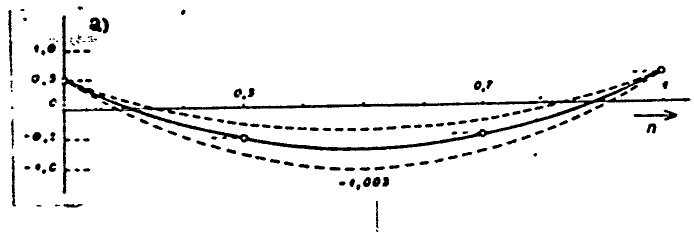

Fig.11 - Less Unfavorable Course of Tabular Error (Solid Line) and Superposed with Coefficient Error (Dotted Line). However, the Sum of the Two Errors Is More Unfavorable Than in Fig.10.

a) In unit of last place

not entered in the Table or perforated in the corresponding tabulated cards.

3.1 Calculation of Interpolation Coefficients. The values of the functions for the binary tabulation arguments (x_r, y_s) are denoted $F_{r;s}$ $(r = 0, 1, 2, \ldots, s = 0, 1, 2, \ldots)$. The values of the functions for the arguments lying between the tabulation arguments (inside the interpolation interval) are denoted $F_{r+n,s+p}$,

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where $0 < n < 1$, $0 < p < 1$. Assume, for example, that in the direction of the argument x there is satisfied the "interpolation on the basis of the interval value" of the 2nd degree and in the direction of the argument y the interpolation of the 3rd degree. For calculating the interpolation coefficients for the parts of the interpolation interval $[(x_r, x_{r+1}), (y_s, y_{s+1})]$ the following functional values must be known

$$\begin{array}{c|cccc} y & & & & \\ \hline & F_{r;s} & F_{r;s+0.3} & F_{r;s+0.7} & F_{r;s+1} \\ & F_{r+0.5;s} & F_{r+0.5;s+0.3} & F_{r+0.5;s+0.7} & F_{r+0.5;s+1} \\ & F_{r+1;s} & F_{r+1;s+0.3} & F_{r+1;s+0.7} & F_{r+1;s+1} \end{array} \tag{3.1}$$

First we calculated for the functional values entered in the first column of the matrices listed above the interpolation coefficients for interpolation in direction h according to eqs.(2.18), (2.19), (2.20). For the values $F_{r;s}$ the corresponding coefficients are calculated from the values present in the first line of matrices,

$$\begin{aligned} a_{0;3} &= [100(F_{r;s+1} - F_{r;s}) - 250(F_{r;s+0.7} - F_{r;s+0.3})]/21, \\ a_{0;2} &= [-100(F_{r;s+1} - F_{r;s}) - 100(F_{r;s+0.3} - F_{r;s}) + 325(F_{r;s+0.7} - \\ &\quad - F_{r;s+0.3})]/21, \\ a_{0;1} &= F_{r;s+1} - F_{r;s} - a_{0;2} - a_{0;3}. \end{aligned} \tag{3.2}$$

Similarly, we calculate for $F_{r+0.5;s}$ from the second line of matrices the coefficients $a_{1,3}$, $a_{1;2}$, $a_{1;1}$, and for $F_{r+1;s}$ from the third line the coefficients $a_{2;3}$, $a_{2;2}$, $a_{2;1}$.

These coefficients form with the corresponding functional values the following matrices

$$\begin{array}{c|cccc} y & & & & \\ \hline & F_{r;s} & a_{0;1} & a_{0;2} & a_{0;3} \\ & F_{r+0.5;s} & a_{1;1} & a_{1;2} & a_{1;3} \\ & F_{r+1;s} & a_{2;1} & a_{2;2} & a_{2;3} \end{array} \tag{3.3}$$

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Next we calculate the interpolation coefficients for the values entered on the first line of these matrices in the direction of the variable x (according to eq.[2.12]). For $F_{r;s}$ we calculate the corresponding interpolation coefficients from the values entered in the first column of matrices

$$b_{2;0} = 2\bar{\Delta}_x^2 F_{r;s}$$
$$b_{1;0} = 2\bar{\Delta}_x F_{r;s} - \Delta_x^2 F_{r;s},$$

where

$$\bar{\Delta}_x F_{r;s} = F_{r+0,2;s} - F_{r;s},\ \bar{\Delta}_x^2 F_{r;s} = \bar{\Delta}_x F_{r+0,2;s} - \bar{\Delta}_x F_{r;s}\ (\bar{\Delta}_x F_{r+0,2;s} = F_{r+2;s} - F_{r+0,2;s}).$$

Similarly we calculate for the values $a_{0;1}$ from the values in the second column the coefficients

$$b_{2;1} = 2\bar{\Delta}_x^2 a_{0;1}$$
$$b_{1;1} = 2\bar{\Delta}_x a_{0;1} - \bar{\Delta}_x^2 a_{0;1},$$
$$(\bar{\Delta}_x a_{0;1} = a_{1;1} - a_{0;1},\ \bar{\Delta}_x a_{1;1} = a_{2;1} - a_{1;1},\ \bar{\Delta}_x^2 a_{0;1} = \bar{\Delta}_x a_{1;1} - \Delta_x a_{0;1}),$$

and for the values $a_{0;2}$ and $a_{0;3}$ from the third and fourth columns the coefficients

$$b_{2;2} = 2\bar{\Delta}_x^2 a_{0;2} \qquad b_{2;3} = 2\bar{\Delta}_x a_{0;3}$$
$$b_{1;2} = 2\bar{\Delta}_x a_{0;2} - \bar{\Delta}_x^2 a_{0;2} \qquad b_{1;3} = 2\bar{\Delta}_x a_{0;3} - \bar{\Delta}^2 a_{0;3}.$$

The coefficients are then composed in the final form of the matrices

$$\begin{array}{cccc} & \underline{y} & & \\ x\downarrow & F_{r;s} & a_{0;1} & a_{0;2} & a_{0;3} \\ & b_{1;0} & b_{1;1} & b_{1;2} & b_{1;3} \\ & b_{2;0} & b_{2;1} & b_{2;2} & b_{2;3} \end{array} \qquad (3.4)$$

For each interpolation interval we perforate in one card besides the binary argument (x_r, y_s) the twelve values entered in the corresponding matrices. The whole "Table" therefore contains as many perforated cards as there are selected fundamental values, or, in other words, as there are interpolation parts of the

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interval.

3.2 Execution of Interpolation. For the binary arguments (x_{r+n}, y_{s+p}), $0 \le n < 1$, $0 \le p < 1$, we must calculate by interpolation the corresponding values $F_{r+n;\, s+p}$.

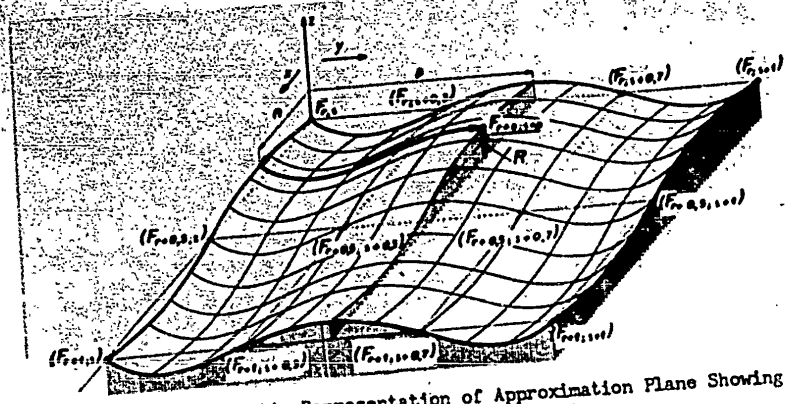

Fig.12 - Schematic Representation of Approximation Plane Showing Location of Interpolation Errors in Parts of Interpolation Interval [(r; r + 1), (s; s + 1)]

Next we calculate for $F_{r;s}$ and the coefficients $a_{0;1}$, $a_{0;2}$, $a_{0;3}$ the corresponding interpolated values in the direction of the variable x.

$$\begin{aligned} F_{r+n;s} &= (b_{2;0}n + b_{1;0})\,n + F_{r;s} \\ a_{n;1} &= (b_{2;1}n + b_{1;1})\,n + a_{0;1} \\ a_{n;2} &= (b_{2;2}n + b_{1;2})\,n + a_{0;2} \\ a_{n;3} &= (b_{2;3}n + b_{1;3})\,n + a_{0;3}. \end{aligned} \tag{3.5}$$

In this way we obtain the functional values $F_{r+n;s}$ and the corresponding interpolation coefficients $a_{n;1}$, $a_{n;2}$, $a_{n;3}$. The calculation is completed by carrying out the interpolation in direction y.

$$F_{r+n;s+p} = ((a_{n;3}p + a_{n;2})\,p + a_{n;1})\,p + F_{r+n;s}. \tag{3.6}$$

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$\sinh(x + iq) = u + iv, \ (q = 2y/\pi)$

q	x = 1						x = 1.1					
	u			v			u			v		
0,0	—16 8 6 26	—1 80 —10 154 19	—14 46 —1 1,175 20	—8 1 32 0	—4 18 42 0	—1 50 242 89 0,009 00	—12 2 7 10	—2 02 —1 166 71	—16 42 —3 1,335 65	8 1 28 0	—20 21 08 0	—1 62 262 63 0,000 00
0,1	—20 —2 6 18	—1 74 —3 91 152 29	—14 10 —28 95 1,160 73	—8 1 32 1 24	—28 18 18 18 38	—4 46 239 91 0,241 59	—24 0 7 00	—1 84 —4 30 164 66	—16 04 —32 38 1,319 20	—8 1 40 1 36	—36 20 66 20 88	—4 82 259 41 0,261 01
0,2	—8 —68 5 96	—1 76 —7 12 146 64	—15 38 —57 19 1,117 68	0 1 16 2 48	—64 17 66 36 28	—7 26 230 97 0,476 84	—4 —38 6 76	—1 94 —8 07 158 54	—15 22 —64 99 1,270 28	—12 1 38 2 68	—54 19 89 41 24	—7 90 249 79 0,515 60
0,3	0 —52 5 00	—1 62 —10 92 137 36	—12 34 —84 01 1,047 11	—12 1 18 3 64	—70 16 43 53 30	—9 94 216 39 0,708 55	—12 —46 6 34	—1 70 —11 97 148 53	—14 06 —95 45 1,190 07	—8 1 24 3 94	—84 18 70 60 59	—10 76 234 00 0,757 40
0,4	—8 —56 5 06	—1 44 —14 26 124 72	—11 02 —108 75 0,980 76	—12 1 10 4 70	—90 14 89 69 03	—12 36 196 48 0,907 00	—8 —64 5 76	—1 56 —15 44 134 86	—12 54 —123 57 1,080 56	—16 1 20 5 10	—96 16 88 78 45	—13 38 212 47 0,980 73
0,5	12 —86 4 44	—1 38 —17 03 109 02	—9 40 —130 82 0,836 99	—16 96 5 66	—1 00 12 98 83 02	—14 48 171 74 1,091 12	0 —84 5 04	—1 44 —18 46 117 86	—10 66 —148 71 0,944 45	—16 1 04 6 14	—1 20 14 80 94 37	—15 64 185 68 1,179 82
0,6	4 —90 3 70	—1 06 —19 55 90 61	—7 56 —149 68 0,690 77	—8 76 6 48	—1 28 10 88 95 00	—16 20 142 72 1,248 38	—4 —94 4 20	—1 10 —21 17 97 96	—8 58 —170 13 0,705 08	—16 88 7 02	—1 32 12 26 107 97	—17 56 154 36 1,349 86
0,7	0 —88 2 84	—76 —21 62 70 00	—5 54 —164 83 0,533 53	—12 58 7 16	—1 34 8 41 104 80	—17 56 110 22 1,374 90	0 —1 00 3 22	—84 —23 36 75 69	—6 30 —187 33 0,606 37	0 52 7 74	1 60 9 62 118 91	—19 02 119 21 1,486 66
0,8	0 —1 00 1 96	—44 —23 04 47 62	—3 40 —175 92 0,363 16	—20 50 7 62	—1 30 5 61 111 67	—18 52 75 04 1,476 56	—8 —1 04 2 22	—44 —24 96 51 49	—3 84 —199 96 0,412 74	—12 4 8 26	—1 58 6 43 126 93	—20 02 81 15 1,506 85

Fig.13 - Example of Table of Sin h (x + iq) = u + iv

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0.9	0 —96 96	—12 —24 02 24 14	—1 16 —182 68 0,183 84	0 12 7 92	—1 52 2 94 115 98	—18 96 37 96 1,524 08	—4 —1 06 1 10	—14 —25 95 26 09	—1 28 —207 66 0,208 94	8 4 8 60	—1 84 3 48 131 78	—20 48 41 02 1,647 98
1.0	0 —96 0	12 —24 26 0	1 16 —185 00 0,000 00	0 —12 8 04	—1 52 10 117 40	—18 96 —4 1,543 08	4 —1 14 0	14 —26 23 0	1 28 —210 22 0,000 00	8 —20 8 72	—1 84 29 133 42	—20 48 —6 1,666 52
1.1	0 —1 00 —96	44 —23 92 —24 11	3 40 —182 72 —0,183 84	—20 —10 7 92	—1 30 —3 01 115 98	—18 52 —38 00 1,524 08	8 —1 20 —1 10	44 —25 84 —26 09	3 84 —207 61 —0,208 94	—12 —22 8 60	—1 58 —3 27 131 76	—20 02 —41 11 1,647 98
1.2	0 —88 —1 96	76 —23 11 —17 62	5 34 —175 91 —0,363 16	—12 —34 7 62	—1 34 —5 73 111 67	—17 56 —75 10 1,467 56	0 —1 00 —2 22	84 —25 01 —51 49	6 30 —199 93 —0,412 74	0 —32 8 26	—1 60 —6 42 126 93	—19 02 —81 17 1,516 85
1.3	—4 —82 —2 81	—1 06 —21 67 —70 00	7 56 —164 30 —0,333 53	—8 —60 7 16	—1 28 —8 32 104 60	—16 20 —110 32 1,374 90	4 —1 02 —3 22	110 —23 37 —75 69	8 58 —187 29 —0,606 37	—16 —56 7 74	—1 32 —9 62 118 91	—17 56 —119 21 1,486 66
1.4	—12 —62 —3 70	138 —19 79 —90 61	9 40 —149 62 —0,699 77	—16 —64 6 48	—1 09 —10 98 95 00	—14 48 —142 78 1,248 38	0 —84 —4 20	144 —21 34 —97 96	10 66 —170 03 —0,785 08	—16 —72 7 02	—1 20 —12 40 107 97	—15 64 —151 40 1,349 86
1.5	+8 —72 —4 14	144 —17 14 —109 02	11 02 —130 79 —0,830 99	—12 —86 5 68	—90 —13 09 83 02	—12 36 —171 76 1,091 12	8 —80 —5 04	156 —18 56 —117 86	12 54 —148 65 —0,944 45	—16 —88 6 14	—96 —14 96 94 37	—13 38 —185 71 1,179 82
1.6	0 —52 —5 08	172 —14 36 —121 72	12 34 —108 69 —0,930 76	—12 —94 4 70	—70 —15 03 69 03	—9 94 —196 51 0,907 00	12 —70 —5 76	170 —15 37 —131 86	14 06 —123 37 —1,000 56	—8 —92 5 10	—84 —17 10 78 45	—10 76 —212 48 0,900 73
1.7	8 —44 —5 60	176 —11 01 —137 36	15 38 —83 95 —1,047 11	0 —1 16 3 64	—64 —16 38 53 30	—7 26 —216 45 0,700 55	4 —46 —6 34	194 —11 95 —148 53	15 22 —95 43 —1,190 07	—12 —114 3 94	—54 —18 81 60 59	—7 90 —233 90 0,457 49
1.8	20 —42 —5 96	174 —7 39 —146 64	14 10 —57 15 —1,117 68	—8 —1 16 2 48	—28 —17 62 36 28	—1 46 —230 99 0,476 84	24 —18 —6 76	184 —7 98 —158 54	16 04 —64 96 —1,270 28	—8 —124 2 68	—36 —20 04 41 24	—1 82 —219 77 0,515 60
1.9	16 —24 —5 18	180 —3 70 —152 29	14 46 —28 93 —1,160 73	—8 —1 16 1 24	—4 —18 34 18 38	—1 50 —239 89 0,241 39	12 22 —7 00	202 —4 05 —164 68	16 42 —32 87 —1,319 20	8 —112 1 36	—20 —20 68 20 88	—1 62 —259 39 0,261 01

$\sinh(x + iq) = u + iv$

Fig.13 - (cont'd)

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The whole calculation is very simple not only when employing machines for processing perforated cards but also when employing printed Tables and a desk computer, provided that the employed Table of functional values also contains the necessary interpolation coefficients.

During the preparation of such a Table we usually start with existing detailed (in extent) Tables and as required determine the width of the interpolation interval and the degree of the interpolation formula in the directions of the variables x and y. With this the fundamental values of the arguments and the corresponding values of the function are also determined. For calculating the interpolation coefficients we use some additional "internal" functional values, which, however, we do not enter in the stock Tables. Finally, the calculation matrices of the interpolation coefficients are arranged in such a way that the individual coefficients follow each other in the same order as they are selected at the execution of the interpolation. Then, for example, the matrices (3.4) are entered in the form of

$$\begin{array}{cccccc} & y & & & & \\ x & b_{2;3} & b_{2;2} & b_{2;1} & b_{2;0} & \\ & b_{1;3} & b_{1;2} & b_{1;1} & b_{1;0} & \\ & a_{0;3} & a_{0;2} & a_{0;1} & \underline{F_{r;s}} & \end{array} \qquad (3.7)$$

Figure 12 schematically represents one part of the interpolation interval for the functional values $F_{r;s}$. For the sake of simplicity $F(x,y)$ is represented as a plane passing through 12 points, denoted by small circles. The values in parentheses are not tabulated; they were used only for calculating the interpolation coefficients occurring in eqs.(3.5) and (3.6). The approximate areas given by eqs.(3.5) and (3.6) for $0 \leq n \leq 1$ and for $0 \leq p \leq 1$ are indicated by the networks. From the depiction the interpolation error is distributed over the whole part of the interpolation interval. In the given scale for z (1 cm = 0.0013), of course, the interpolation error when approximating $F(x,y)$ can only occur if

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$$\frac{\partial^3 F(\xi, y)}{\partial x^3} = \frac{1}{20h^3} \text{ and } \frac{\partial^4 F(x, \eta)}{\partial y^4} = \frac{1}{k^4}, \text{ where } h = x_{r+1} - x_r$$
$$\text{and } k = y_{s+1} - y_s;\ x_r < \xi < x_{r+1} \text{ and } y_s < \eta < y_{s+1}.$$

The graphical representation of the function X_i of the equation for the interpolation error at one independent variable is analogous.

For example, in the Table of the functions of two independent variables of Fig.13 we give on one side of the Table of sin h (x + iq) in the interval for x = = 1.0 to 1.2 and for $q = \frac{2y}{\pi}$ = 0.0 to 2.0. Also we carry out here the interpolation with the values which are given at one or more places in order not to burden the precision of the result with the tabulation and rounding errors.

Example: We have to find the value of sinh $(1.150 + 1.3352\ i)_y$. In order to be able to use the Table of Fig.13 we first convert the value y = 1.3352 to q according to the relation $q = \frac{2y}{\pi}$, so that q = 0.850.

$$\sinh(1.150 + 1.3352\ i), \quad \sinh(1.150 + 0.850\ i), .$$

In the Table (Fig.13) we find for the arguments x = 1.1 and q = 0.8 the corresponding interpolation coefficient for calculating u and v.

u:

$$\overset{n}{(-8 \times 0{,}5 - 44)} \times \overset{n}{0{,}5} - 3\ 84 = 4\ 08$$
$$(-1\ 04 \times 0{,}5 - 24\ 96) \times 0{,}5 - 199\ 96 = -212\ 70$$
$$(2\ 22 \times 0{,}5 + 51\ 49) \times 0{,}5 + 0{,}412\ 74 = 0{,}439\ 04$$

$$\overset{p}{(-4\ 08 \times 0{,}5 - 212\ 70)} \times \overset{p}{0{,}5} + 0{,}439\ 04 = -0{,}331\ 67$$

v:

$$\overset{n}{(-12 \times 0{,}5 - 1\ 58)} \times \overset{n}{0{,}5} - 20\ 02 = -20\ 84$$
$$(46 \times 0{,}5 + 6\ 43) \times 0{,}5 + 81\ 15 = 84\ 48$$
$$(8\ 26 \times 0{,}5 + 125\ 93) \times 0{,}5 + 1{,}586\ 85 = 1{,}652\ 38$$

$$\overset{p}{(-20\ 84 \times 0{,}5 + 84\ 48)} \times \overset{p}{0{,}5} + 1{,}652\ 38 = 1{,}689\ 41 = v$$

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Result:

$$\sinh(1.150 + 1.3532\,i) = 0.3317 + 1.689\,i^{*})$$

Similarly, as with the functions of two independent variables, it also is possible to calculate the interpolation functions for Tables greater than two-dimensional. The interpolation of these interpolation coefficients can therefore be carried out relatively easy in supplementary multidimensional Tables.

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Remarks of Editorial Board on Treatise of J.M.Marek

This treatise is written, as it were, exclusively from the viewpoint of the rationalization of interpolations on the calculation perforator, so that it touches only in passing, if at all on the great importance of presented Tables on this kind of interpolation to the national economy and of their importance to the simplification of scientific works.

Their national-economic importance follows from the fact that the contents of the Tables, thanks to this interpolation, can be reduced to 1/2 at employment of

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* The interpolation error in this point is zero because the point passes through the approximational surface.

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interpolations of the 2nd degree and to 1/3 at employment of interpolations of the 3rd degree (interpolations of still higher degree almost never occur in the practice), at which the Tables of the functions for interpolations of the 2nd and 3rd degrees give in both cases results approximately precise to the 10th place. Moreover, the employment of this new interpolation wholly eliminates the auxiliary Tables of the coefficients of the interpolation formulas necessary for simplifying the work with the previous interpolation methods. From this follows a saving in the printing of such Tables, with a considerable decrease in the cost of such Tables.

From this it follows further that a considerably larger number of people will be able to procure and use these considerably cheaper Tables, with whose help they will be able to simplify and rationalize their scientific work, also at the employment of only desk computers.

We think that this aspect of the matter is very important.

SUMMARY

The article discusses a method of interpolating functions of one or more independent variables by the use of punched-card or other computing machines. In Chapter I, a survey is given of the most important interpolation formulas. In Chap.2, an interpolation formula is presented which is derived on the basis of the (untabulated) values of the function within the interpolation interval. The precision of the approximation is i^{i+1} times greater than that of the Newton formula, where i is the degree of the interpolation polynomial. Errors of interpolation, tabulation and coefficient are discussed. In Chap.3, the formula for interpolation of functions of two independent variables is presented, and as an example, one page of the tables for $\cosh(x + iq)$, where $q = \frac{2y}{\pi}$. The article shows how simple the method is for two-dimensional tables containing the necessary interpolation coefficients.

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SOLUTION OF FIRST BOUNDARY PROBLEM OF LAPLACE'S EQUATION ON MACHINE FOR PERFORATED CARDS*

by

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Received: November 24, 1953

1. Introduction

Boundary problems of partial differential equations usually lend themselves conveniently to analytical solution only for regions of very simple geometrical form. With regions of more complicated form an analytical solution often encounters enormous difficulties, so that often only calculation according to suitable numerical methods leads to the goal. One such method which has been found particularly useful for such problems is the method of networks, where a connected problem replaces an unconnected problem. Its advantages are its calculating simplicity, objectiveness, the possibility of applying it to regions of very general form, and finally, the fact that it gives us an approximate knowledge of the solution (first approximation) often enables a considerable decrease in the effort put into the numerical solution.

When, however, it is desired to obtain a highly-precise result, this method usually leads to very voluminous calculations, so that in this case it is better to use a mathematical machine. Insofar as I know, the first attempts in this direction, the solution of the first boundary problem of Laplace's equation, were undertaken

* Presented to the Second Regular All-State Conference of the Laboratory of Mathematical Machines in December 1953.

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on the machines for perforated cards of the Powers system and of the Kormes-IBM system (Bibl.12). Another experiment was carried out on the Soviet machine for perforated cards (Bibl.11). However, both of these methods would have had to be modified for our type of machine. Moreover, they are suitable only for regions of very simple form. We present below an example of the solution of the first boundary problem of Laplace's solution as it can be carried out on the Aritma calculation perforator.

2. Mathematical Formulation of Problem

Let G be a simple continuous region of a real plane (x,y) delimited by the closed line C. We seek the function v(x,y) which in this region satisfies the equation

$$\frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} = 0 \qquad (1)$$

and which is connected in the closure $\bar{G} = G + C$ of the region and acquires a given value on the boundary C. Assume that the given value is such that the sought function exists.

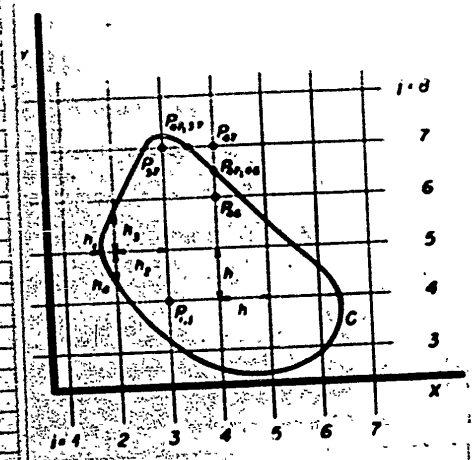

Fig.1

The essence of the method of networks consists in that the differential equation is replaced with a difference equation, which, as is known, is obtained from the differential equation in that the derivations and the various kinds of differential operations are replaced with their difference approximations.

Parallel with the coordinate axis (see Fig.1) we laid through the region G

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two axial parallels forming a square network whose "sides", i.e., distances between the neighboring parallels, we denote h. The intersections of the two axial parallels lying inside C will be called the internal points of the network. The intersection of the ith axial straight parallel with axis Y and the jth axial straight parallel with the axis X will de denoted P_{ij}. The intersection of the two axes with C will be called the boundary point of the network. In it the value v is given. The lenghts h of the sides of the network are selected sufficiently small that the internal points of the network form a "continuous region"*. Next, inside C we form the proportional difference by which we approximate eq.(1). Let the network function u(n,y) which is approximation of the function v, acquire in any internal point of the network P_{ij} the value u and in four neighboring points $P_{i+1,j}P_{i-1,j}P_{i,j+1}P_{i,j-1}$ the values $u_{i+1,j}u_{i-1,j}u_{i,j+1}i_{i,j-1}$. If at some side of the network starting at the point $P_{i,j}$ and going, for example, to the point $P_{i,j+1}$ intersects the line C, we denote this intersection $P_{i,j+1;i,j}$ and lay it in the same direction from the neighboring point relative to P_{ij}. The value of u is given in it and is denoted $u_{i,j+1;ij}$ (the second double index distinguishes this value, for example from the values $u_{i,j+1;i-1,j+1}$ in the intersections $P_{i,j+1;i-1,j+1}$ of the curve C of the joining lines $P_{i-1,j+1}$ $P_{i,j+1}$). The value $u_{i,j+1}$ corresponding to the external point of the network $P_{i,j+1}$ does not occur in our calculation. While it is included in this figure of the considered network, there is danger of confusing it with the number and the point, so that hereafter we shall usually omit this second double index in the denotation of the functions as well as in the denotation of the points. The distance between the points

$P_{ij}P_{i-1,j}$ is denoted h_1

$P_{i+1,j}P_{ij}$ is denoted h_2

---

* That is, for every two interval points PP* which are not neighboring (see below) exists such a sequence of the internal points of the network P, P_1, P_2,.. P_n, P* that every two points following each other are neighboring.

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$P_{i,j+1}P_{ij}$ is denoted h_3

$P_{ij}P_{i,j-1}$ is denoted h_4

(h_1, h_2, h_3, h_4 can differ from each other only when some of the given points P are boundary points).

The first and second partial difference shares in the point P_{ij} are therefore the expressions

$$\frac{u_{i+1,j} - u_{i-1,j}}{h_1 + h_2} \cdot 2\frac{u_{i+1,j}}{h_1(h_1 + h_2)} - 2\frac{u_{ij}}{h_1 h_2} + 2\frac{u_{i-1,j}}{h_2(h_1 + h_2)}$$

$$\frac{u_{i,j+1} - u_{i,j-1}}{h_3 + h_4} \cdot 2\frac{u_{i,j+1}}{h_3(h_3 + h_4)} - 2\frac{u_{ij}}{h_3 h_4} + 2\frac{u_{i,j-1}}{h_4(h_3 + h_4)}. \qquad (2)$$

Substitution in eq.(1) of the partial derivative of these expressions gives, after preparation, the difference equation

$$a_{ij}u_{i+1,j} + b_{ij}u_{i-1,j} + c_{ij}u_{i,j+1} + d_{ij}u_{i,j-1} - u_{ij}. \qquad (3)$$

a_{ij}, b_{ij}, v_{ij}, d_{ij} are constants (i, j run through the indexes of all of the internal points of the network). Equation (3) forms a system of linear equations with the same number of equations and unknowns. While various methods for the solution of this system exist, we shall hereafter, in order to be able to employ the machine for perforated cards, use the iterative method of Richardson with correction on the boundary of the region G (for which the numerical procedures employed are known, for example, in electrotechnology at the calculation of electrostatic fields: The value u in each point of the network is replaced with the arithmetical average values in four neighboring points; when we replace all of the points of the network we begin again at the beginning). For the internal points of the network all of whose neighboring points are likewise internal points of the network, eq.(3) really has the form of

$$\frac{u_{i+1,j} + u_{i-1,j} + u_{i,j+1} + u_{i,j-1}}{4} = u_{ij}.$$

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The initial approximation of u_{ij} is denoted $u_{ij}^{(0)}$; the value obtained by the kth iterative step is denoted $u_{ij}^{(k)}$.

3. Planning of Calculation for Machine for Perforated Cards

Next we describe in detail the planning of the whole calculation for the machine for perforated cards.

3.1 Some Terms Used for Calculation with Perforated Cards. A clear description of the machine for perforated cards and an introduction to the method of planning technical calculations are presented in "Machines for Processing Information, Collection I, Mathematical Machines". Here we shall recall only some terms and word pictures which will occur below.

A column of a card in which a number or an index is entered, is called a "field". Such fields are denoted by capital letters, for example, P, Q, A_0, A_1, A_2. If, in the course of a calculation all of the fields of the cards are occupied, we replace these cards with new ones, with which we continue the calculation. This new set of cards is called the "new set", to distinguish it from the original set with which the calculation was begun. The cards of the two sets are distinguished by an index perforated in one of the index fields. The calculation is carried out with one or several "packs" of cards, which are identified by Roman digits. "Pack I placed before Pack II and both arranged according to ascending index in field Q" means that the cards are arranged according to the ascending index in the field Q, and in such a way that in case of the same index on the cards of packs I and II the cards of pack I go ahead of the cards of pack II.

We shall assume the employment of the calculation perforator, which is put out by Arithma in the standard model for mathematical work and in a small model, which makes this machine suitable for carrying out technical calculations. Contrary to the standard model, only this arrangement is further assumed: For saving the sum the machine does not save the value from the main card - the intermediate result and the result saved may also be negative.

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3.2 Division of Fields on Cards. - The columns of the cards are divided into a number of fields which according to the purpose are denoted by letters as follows:

P, Q, R ..... denote index fields

A_k for $k = 0, 1, 2, \ldots, n$ ..... denotes the calculation field

K ..... denotes a constant field

To each internal point P_{ij} of the network correspond five cards having the indexes i, j in the field P. One of them has the perforation of the main card, the others are ordinary. The cards with the perforation of the main card for all of the internal points of the network form pack I. The remaining cards form pack II. On the cards of pack I the same index as in P is in the field Q. On the cards of pack II the same indexes i, j are always on the four cards in the field P, but the cards differ from each other in the field Q by the indexes, which are: i + 1,j; i - 1,j; i,j + 1; i,j - 1. In the field R is the number of the problem to be solved (several of them are solved at the same time) and the number of the set. Beginning with the evaluation of $u_{ij}^{(0)}$ we perforate in the cards of pack I only the first calculation field A_0. The remaining fields A_i in the pack I remain empty for the time being. On the cards of pack II, besides the mentioned fields, the field of K carrying the constants from eq.(3) are also carried. The following are placed on the cards:

a_{ij} is on the card which has in the field P the index ij and in the field Q the index i + 1,j

b_{ij} is on the card which has in the field P the index ij and in the field Q the index i - 1,j

c_{ij} is on the card which has in the field P the index ij and in the field Q the index i,j + 1

d_{ij} is on the card which has in the field P the index ij and in the field Q the index i,j - 1

If, however, the point $P_{i+1,j}$ (or $P_{i-1,j}, P_{i,j+1}, P_{i,j+1}, P_{i,j-1}$) is a bound

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point), i.e., if $u_{i+1,j}$ (or $u_{i-1,j}$, $u_{i,j+1}$, $u_{i,j-1}$) is known, then the field K contains zero, and in all of the fields A_i is perforated the known value of the product $u_{i+1,j}d_{ij}$ (or of $u_{i-1,j}b_{ij}$, etc) also with the perforation of correctness.

A survey of the scheme of the perforating is given in Fig.2, which represents one of the internal points of the network all of whose neighboring points are likewise internal.

The effort connected with the calculation of the constants q_{ij}, b_{ij}, c_{ij}, d_{ij}, which may at first glance seem considerable, is actually no greater than at calculation on the calculator.

3.3 Sequence of Operations. The kth iterative step is carried out as follows:

1. The cards of pack I are placed ahead of the cards of pack II, and both packs are arranged in the order of ascending index in the field Q.

2. We carry out multiplication with the main card, i.e., with the main card we take the field A_{k-1} and with the ordinary card the field K. In this way we form the numbers $a_{i-1,j}u_{ij}^{(k-1)}$, $b_{i+1,j}u_{ij}^{(k-1)}$, $c_{i,j-1}u_{ij}^{(k-1)}$, $d_{i,j+1}u_{ij}^{(k-1)}$. (This operation for the point P_{ij} is indicated by the solid arrows in Fig.2.)

3. The cards of packs I and II are sorted (for example, by sorting according to the perforation of the main cards. Then pack II is placed ahead of pack I, and both are arranged in the order of ascending index in the field P.

4. We carry out the operation of "saving the sums" from the field A_{k-1} - the sums are perforated in the field A_k of the main cards, i.e., in the cards of pack I. In this way we form:

$$a_{ij}u_{i+1,j}^{(k-1)} + b_{ij}u_{i-1,j}^{(k-1)} + c_{ij}u_{i,j+1}^{(k-1)} + d_{ij}u_{ij-1}^{(k-1)} \quad u_{ij}^{(k)}$$

This operation for the point P_{ij} is indicated by the broken arrows in Fig.2. Then in the field A_k in the cards of pack I the value of $u_{ij}^{(k)}$ is calculated, obtained by the kth iterative step.

Then for the whole calculation this operation is repeated in cycles. From

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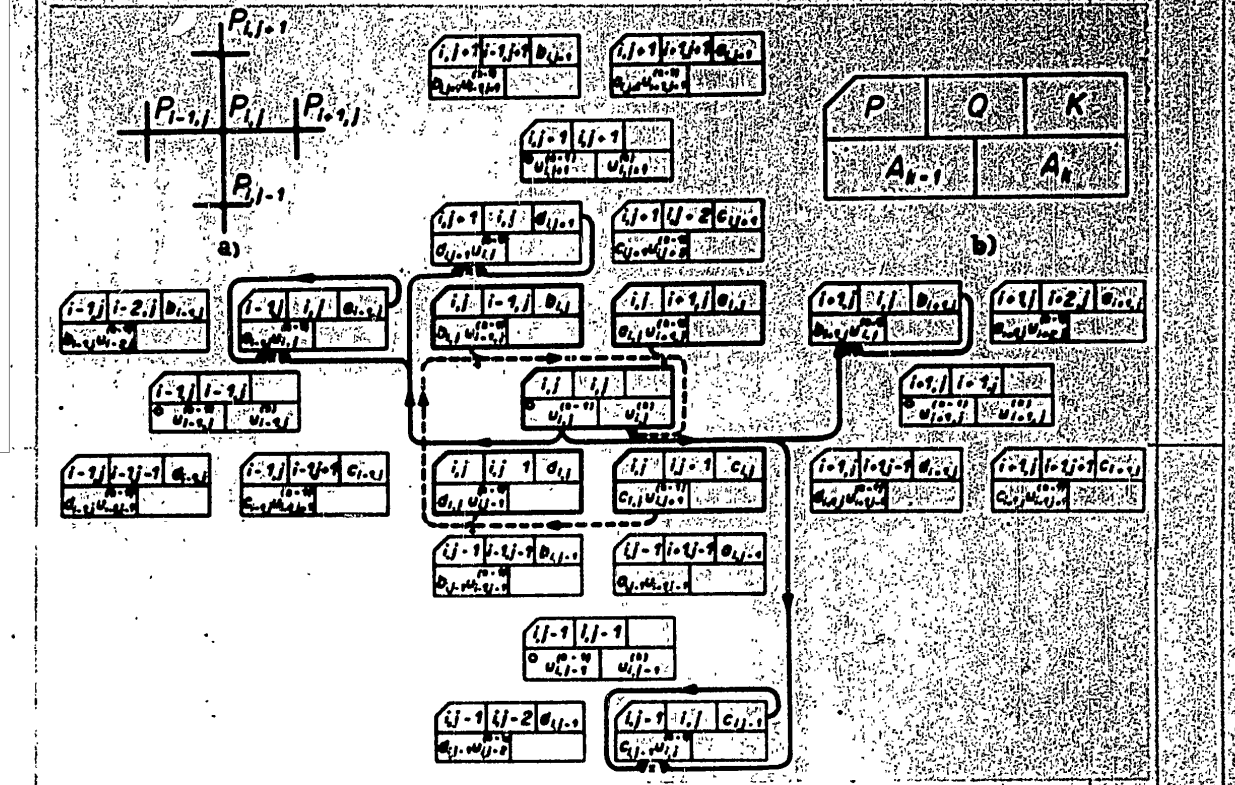

Fig.2 – Scheme of Calculation

a) Difference network around point i,j; b) Arrangement of fields on cards

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time to time the values of $u_j^{(k)}$ from the pack I are printed on the tabulator for ascertaining whether the iteration should be terminated.

If the field A_k on all of the cards is already occupied we take for operation 1 instead of the occupied pack II a new pack II. The cards of this new set have in the fields P, Q, K the same indexes as the cards of the original set, and differ from the latter only by a different set in the field R. Then in operation (3) we use an analogously-preperforated new set of pack I. The rest of the procedure is exactly the same as above.

3.4 Some Remarks on Practical Execution of Calculations. In order for the above-described employment of the machine for perforated cards to be sufficiently efficient, it is advisable to solve with it only problems whose networks have a sufficiently large number of internal points - at least 100. Problems with networks with a smaller number of points could not be efficiently solved by this method; the number of cards is here too small and the expenditure of time too great with the present model of the machine.

If with Laplace's equation a rectangular region is concerned, it is necessary according to Frankel (Bibl.5) to estimate the number of iterative steps according to the equation

$$\eta \doteq \frac{6}{\log\left(1 - \frac{\pi^2}{4}\left[(p+1)^{-2} + (q+1)^{-2}\right]\right)}$$

where p and q are respectively the internal points of the network in the longitudinal and transverse directions of the rectangular region. If the maximal permissible error at the first approximation is ε then at η steps this error must be reduced to a value smaller than $\varepsilon \cdot 10^{-6}$.

From this formula it is clear that the number of iterative steps is increased by approximately the second power of the number of internal points. Therefore, it is advisable to find the best possible first approximation, i.e., by several trials, graphically or by the relaxation method, with a network with a small number

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points. If a greater precision is required than at the employment of the method of networks it is usually desirable to use a different formula with remainders of a higher order, which, of course, leads to complication of the calculation (particularly on the boundary), but it is still feasible with a fairly thin network. For the employment of perforated cards this method cannot be regarded as advantageous (except perhaps in some particularly exceptional cases), because here the advantage of the smaller number of arithmetical operations does not outweigh the disadvantage of the complication of the calculating procedure which is most simply carried out with perforated cards. Therefore, if a precision of the result higher than can be obtained with the approximate 100 points of the network is required, we must carry out the calculation with this number of points, and, after finishing it, concentrate the network - for example, use half of the network. At the first approximation for the concentrated network, the arithmetical average of the function u in the closest points of the original network may be used with advantage. This whole procedure can likewise be carried out very easily on the machine for perforated cards.

Several calculating measures which, by enabling convergence, accelerate the above-described iterative procedure (1), (9), are known. These methods of accelerating the convergence can very easily be incorporated with the above-described calculating procedure; the detailed planning is very simple; the reader can easily compose it himself.

4. Generalization

We seek the function c which in the simple continuous region G bounded by the closed line C satisfies the elliptical differential equation in the canonical form [on the transformation of the general elliptical differential equation form, see (Bibl.10)]

$$\frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} + f_1(x, y)\frac{\partial v}{\partial x} + f_2(x, y)\frac{\partial v}{\partial y} + f_3(x, y)\, v = g(x, y)$$

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and which is connected in $\bar{G} = G + C$ and acquires the given value on the boundary C. (We assume that this given value as well as the functions f_1, f_2, f_3 are much that v exists.)

Analogously as with Laplace's equation we replace the partial derivation in eq.(4) with the difference equation (2) and obtain an equation very similar to eq.(3)

$$\bar{a}_{ij}u_{i+1,j} + \bar{b}_{ij}u_{i-1,j} + \bar{c}_{ij}u_{i,j+1} + \bar{d}_{ij}u_{i,j-1} + \bar{e}_{ij} = u_{ij}$$

where in $\bar{a}_{ij}$, $\bar{b}_{ij}$, $\bar{c}_{ij}$, $\bar{d}_{ij}$, $\bar{e}_{ij}$ not only the lengths h_1, h_2, h_3, h_4 are included, but also the values of the functions f_1, f_2, f_3, g.

The planning for the calculation on the machine for perforated cards is substantially the same as with Laplace's equation, only the constant $\bar{e}_{ij}$ is located on the cards with the index ij in the field P of pack I in such a way that it is also added at operation 4. The calculation of the constants $\bar{a}_{ij}$, $\bar{b}_{ij}$, $\bar{c}_{ij}$, $\bar{d}_{ij}$, $\bar{e}_{ij}$, however, makes much more work and requires a very much larger number of perforations. Sometimes, however, it may be advantageous to carry out also this calculation with perforated cards. The planning, therefore, depends on the form of the functions f_1, f_2, f_3, g.

It will also be clear to the reader that the first boundary problem of Laplace's equation for space can be solved similarly. Here to each internal point seven cards correspond, and the rest of the planning remains substantially unchanged. It is likewise clear that the above-described method can also be used for networks of a form other than square - for example, rectangular, triangular, hexagonal, or, for example, for rectangular networks whose sides are not wholly the same as those of the region G.

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SUMMARY

The work concerns the solution of the Laplace equation for boundary conditions of the first kind on punched card computing machines manufactured by national enterprise Aritma. The computation is performed by means of a net using the Richardson iteration method. The present method may be applied not only to regions of simple

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form but, by the use of linear interpolation on the boundaries, may be used on regions of arbitrary shape without any complication and with the same efficiency. The procedure can be modified in various ways to obtain the most rapid convergence, and it may also be applied to the general equation of elliptic form in two independent variables and the Laplace equation for three-dimensional space.

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SYNTHESIS OF RELAY NETWORKS*

by

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1. Introduction

The method of synthesis of relay networks which is outlined in the present work relates at the present time to the most fundamental problem of the construction of relay machines: the design of the individual relay contacts of the network* whose transmissibility is prescribed by Tables. It is, however, hoped that the numerical symbols used in the work besides the expression of Boolian algebra can also be used for the solution of other problems.

The work must not be regarded as an effort to exclude Boolian algebra from the problems of relay circuits, but, on the contrary, with the proposed numerical symbols we get a better idea of the relations between the algebraic expressions, and we can use this idea in the solution of relatively difficult problems.

The fundamental concepts will be defined here only to the extent necessary to avoid confusion. It is assumed that the fundamentals of Boolian algebra and of the synthesis of simple relay networks are known.

The author thanks the members of the collective staff of the Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences for the many fruitful suggestions following from the discussion periods. It should be mentioned that M.Valach and V.Vysin collaborated actively in the solution of some fundamental problems of the described method. The development of the method was also influenced to some extent by the work of F.Svoboda, who in April 1953 pointed out the disadvant-

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* The term "relay circuit" as used, for example, by Gavrilov (Bibl.3), does not apply to our work.

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ages of the expressions of Boolian algebra as a tool for the general synthesis of relay networks. The author thanks M.Valach for useful help in the arrangement of this text.

1.1 Numerical Symbols. For the solution of the problem of the synthesis of relay networks we proposed symbols using sets of whole numbers whose elements are written out in detail. We assume that the reader is familiar with the most fundamental knowledge of definitive sets and with the fundamentals of Boolian algebra (1).

We select the fundamental set I (read "i") of whole numbers. The selection is carried out simply by writing out the element i of this set (for example, i = 0, 1, 2, ..., n - 1). The subsets of the fundamental set are composed exclusively of elements selected from the fundamental set. The subsets formed in this way are denoted by the symbols

$$a, b, \ldots, y, z, \bar{a}, \bar{b}, \ldots, \bar{y}, \bar{z}$$

The empty set is denoted by the symbol $\emptyset$.

The subsets a, b, are equal to each other if each of the elements of a set a is an element of the set b, and each of the elements of the set b is an element of the set a. We write

$$a = b \qquad (1.1;1)$$

The set c is united* with the set a, b if each of the elements of the set a is an element of the set c, if each of the elements of the set b is an element of the set c, and if each of the elements of the set c is an element of the set a or an element of the set b. We write

$$a \cup b = c \qquad (1.1;2)$$

The set d is a penetration of the sets a, b if each of the elements of the

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* In our mathematical literature the same term "united set" also occurs

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common sets a, b is an element of the set d and if each of the elements of the set d is simultaneously an element of both sets a, b. We write

$$a \cap b = d. \qquad (1.1;3)$$

The sets a, b are mutually disjunctive if they have common elements. Their penetration is therefore empty, and we write

$$a \cap b = 0. \qquad (1.1;4)$$

The sets a, b are mutually conjunctive if they occur united with the fundamental set I. We write

$$a \cup b = I. \qquad (1.1;5)$$

The sets a, b are mutually supplementary if they are simultaneously mutually conjunctive and disjunctive, i.e., if simultaneously eqs.(1.1;4) and (1.1;5) are valid. Instead of these two relations we then write more briefly

$$\text{either } a = \bar{b}, \text{ or } \bar{a} = b \qquad (1.1;6)$$

An overlined symbol denotes a set which is supplementary to a set denoted by a nonoverlined symbol.

If two sets are equal to each other, a set which is equal to them occurs at their penetration or at their union:

$$a \cap a = a, \quad a \cup a = a. \qquad (1.1;7)$$

A set which occurs by union, penetration or another operation with a set may enter into union or penetration with another set. The operational procedure at complex operations is denoted by parentheses. The operational procedure can be modified by using some fundamental statements. We present a few examples.

Example 1. Union and penetration are commutative operations. The expression

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$$d = a \cup (b \cap c) \qquad (1.1;8)$$

means that the set d is formed at this operation on the sets a, b, c, previously formed by penetration of the sets b, c; the set formed in this way unites with the set a. It is directly clear that the same set d is formed according to the expression

$$d = a \cup (c \cap b) = (c \cap b) \cup a = (b \cap c) \cup a. \qquad (1.1;9)$$

Example 2. Union and penetration are symmetrically distributive. The expression $e = a \cap (b \cup c)$ can be developed by a method analogous to multiplication of the expressions in parentheses according to the rules of elementary algebra:

$$e = a \cap (b \cup c) = (a \cap b) \cup (a \cap c). \qquad (1.1;10)$$

The analogous expression of ordinary algebra would be $e = a(b + c) = ab + ac$. In ordinary distributive algebra, however, the expression $d = a + bc$ cannot be transformed to the expression $(a + b)(a + c)$. At union and penetration, however, the distributiveness is symmetrical, i.e., the following applies:

$$d = a \cup (b \cap c) = (a \cup b) \cap (a \cup c). \qquad (1.1;11)$$

Example 3. Associativeness of union (penetration). In expressions containing only one type of operation (only union or only penetration) the order in which the sets enter the operation is a matter of indifference. For example

$$f = a \cup (b \cup c) = (a \cup b) \cup c = a \cup b \cup c. \qquad (1.1;12)$$

A similar example could be written for penetration.

Example 4. Absorption of the considered relation, which has no analogy in elementary arithmetic. For each b the following are valid:

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$$g \equiv a \cap (a \cup b) \equiv a, \qquad (1.1;13)$$

$$h \equiv a \cup (a \cap b) \equiv a. \qquad (1.1;14)$$

Example 5. Transformation of the given expression in such a way that the set supplementary to the set originally expressed is obtained. For the assumption that in the expression there are no supplements of whole parentheses, the rule is valid: each symbol of the expression is replaced with its supplement and union and is replaced with penetration and conversely. The supplements of the sets of the given expression (1.1;8, 10, 12) will be for example:

$$d \equiv \bar{a} \cap (\bar{b} \cup \bar{c}), \qquad (1.1;15)$$

$$e \equiv \bar{a} \cup (\bar{b} \cap \bar{c}), \qquad (1.1;16)$$

$$f \equiv \bar{a} \cap \bar{b} \cap \bar{c}. \qquad (1.1;17)$$

Example 6. The course of the operations on the sets is written out in detail.

Fundamental set	$I =$	0 1 2 3 4 5 6 7
Selected subsets	$a =$	0 1 2
	$b =$	0 3 4
	$c =$	2 3 6
Supplements of selected subsets	$\bar{a} =$	3 4 5 6 7
	$\bar{b} =$	1 2 5 6 7
	$\bar{c} =$	0 1 4 5 7
Numbering of eq.(1.1;8):	$(b \cap c) =$	3
	$d = a \cup (b \cap c) =$	0 1 2 3
Direct supplement of this set	$=$	4 5 6 7
Numbering of same sets according to eq.(1.1;15):	$(\bar{b} \cup \bar{c}) =$	0 1 2 4 5 6 7
	$\bar{a} \cap (\bar{b} \cup \bar{c}) =$	4 5 6 7

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The subsets of the given fundamental set are expressed by the general symbols a, b, c, ..., or by numerical symbols, at which the elements of the subsets are written out in detail.

1.2 Boolian Symbols. For the solution of problems in the analysis and synthesis of relay circuits Boolian algebra is widely employed today as a very advantageous expedient. Between the set-form numerical symbols described in the preceding chapter and between the variables of Boolian algebra we propose relations which lead to a certain isomorphism of the set-form and the Boolian expressions. The derived set-form expression can therefore be directly interpreted according to Boolian algebra and conversely. With this we have the assurance that we can utilize all of the artifices from Boolian and at the same time some new artifices which enable us to introduce numerical symbols.

We have the fundamental numerical set I and some of its subsets a. Concerning every element i of the fundamental set I it can be said that

"the element i is an element of the set a".

This statement is true only for those elements i which belong to the set a. For the remaining elements of the set I it is untrue.

We introduce the variable a' expressing the correctness of the above statement. With the correct statement let a' = 1, with the incorrect statement let a' = 0. With these values of the statement we also introduce the elements of the sets b, c, ..., and denote them b', c', ...

If the set c equals the united set a, b eq.(1.1;2) is valid. The consequence of this relation between the sets a, b, c is the relation between the values a', b', c', of the corresponding statement expressed by the expressions of Boolian algebra.

If an element i is not an element of either the set a or the set b, then neither is it an element of the set c. Therefore, at a' = b' = 0 we have c' = 0.

If an element is an element of either the set a or the set b or of both

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it is also an element of the set c. Therefore, for a = 1, b' = 0 or for a' = 0, b' = 1 or for a' = b' = 1, c' = 1 is valid.

Expressed by Tables:

a'	b'	c'
0	0	0
1	0	1
0	1	1
1	1	1

These Tables agree with the Tables for addition according to two-value Boolian algebra. Employment of this algebra for expressing the relation between the values a', b' gives

$$c' = a' + b' \text{ at the relation } c \equiv a \cup b \quad (1.2;3)$$

a'	b'	d'
0	0	0
1	0	0
0	1	0
1	1	1

If the set d is a penetration of the sets a, b eq.(1.1;3) is valid. The found relation between the values a', b', d' eq.(1.2;1) shows therefore that an element i is an element of the set d(d' = 1) only if it is at the same time also an element of both sets a and b (a' = 1, b' = 1). The Tables expressing this dependence therefore agree with the Tables for ordinary multiplication and with the Tables for multiplication according to Boolian two-value algebra. Therefore

$$d' = a'b', \qquad d \equiv a \cap b. \qquad (1.2;4)$$

If the sets a, b are supplementary and we seek the relation between the corresponding values a', b' we find for eqs.(1.1;4) and (1.1;5) the following relations

$$\begin{aligned} a'b' &= 0, \text{ if } a \cap b \equiv 0, \\ a' + b' &= 1, \text{ if } a \cup b \equiv I. \end{aligned} \qquad (1.2;5)$$

Detailed analysis leads to the conclusion that the expressions written in the form of sets are isomorphous with the expressions of Boolian algebra for the values of expressions of the form of (1.2;1), as shown by the following Table.

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In the next chapter we will use such statement-form and set-form symbols that the isomorphism is nowhere disturbed. For avoiding misunderstandings, therefore, we arrange the symbols for employment in the next chapter as follows: We put a at the statement element, i.e., the symbol a, for example, sometimes means the value of the statement and other times the set of the number corresponding to it in the sense of isomorphism.

a) Values of statement of element i	b) Set of element i
$a', b', \ldots$	$a, b, \ldots$
$+$	$\cup$
$\cdot$	$\cap$
$=$	$\equiv$

A united set is expressed by the plus sign the same as the sum of two statement values. A penetration is written the same as the product of two statement values. The sign of equality is used for expressing the functional value of the statement. The symbol of identity is used for expressing agreement between two sets (which usually corresponds to identity between two functions).

In the above-described sense, therefore, for example

$$a = 0, \quad b = 1, \tag{1.2;7}$$

denote the functional values of the statement functions. On the contrary, the expressions

$$a \equiv \emptyset, \quad b \equiv I \tag{1.2;8}$$

mean that the numerical set a is empty (the corresponding statement value is equal to zero identically for all values of the independent variables) and that the set b is equal to the fundamental set I (the corresponding statement values are identically equal to 1).

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2. Switch Signal Networks

The signal network (Fig.1) is composed of the nodes M, N, P, ..., between which signals are provided through the intermediary of the signal conductors MN, MP, ..., NP, ..., and concerning which signal transmissibility in both directions along the conductors is assumed.

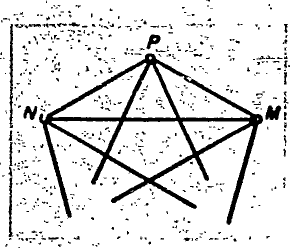

Fig.1 - Signal Network

With a switch signal network the transmissibilities of the individual conductors are dominated by switches. If the latter are contacts which connect and disconnect through the intermediary of electromagnetic relays we have relay switches (see Chapters 2.1 and 2.3) and a relay contact network. We shall hereafter, for the sake of brevity, call such a network a relay network.

A relay network is composed of a fairly large number of relays. Some of these relays are interdependent, usually because their windings are connected in parallel or in series. It is therefore clear that they are simultaneously in agreement in state (resting or working) and that they are governed solely by the signal conductors. A relay network which is governed by a common signal circuit is denoted by common marks such as A, B, C, ... The states of the corresponding signal circuits are expressed by the values of the variables a, b, c, ... according to which

$$a = 0,\ b = 0,\ \ldots,\ \text{etc.}$$

mean that the signal circuit and its corresponding relay are in the resting state, and

$$a = 1,\ b = 1,\ \ldots,\ \text{etc.}$$

mean that the signal circuit and its corresponding relay are in the working state.

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The governor of the signals of the relay network is composed of signal com-

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ponents. The latter are the impulses of the individual signal circuits of the relay group A, B, C, ... In extending the sense of the word we denote the signal components by the same variables a, b, c, ... The governor of the signals of the network is therefore symbolized by a system of values of the same variables. Every possible system of unities and zeros corresponds to a different system of impulses of the governed signals, a different combination of states of the relays (relay group A, B, ...), and hence also a different working state of the network.

A switch signal network whose signal governor has m components can acquire 2m different working states. These states may be listed in a Table, in which each line corresponds to one state of the network corresponding to one of the combinations of the values of the components of the governed signals.

Example 7. The signal governor has three components a, b, c. Therefore, the Table of all possible working states has eight lines, as follows:

We define the state index i by the relation

$$i = a \cdot 2^0 + b \cdot 2^1 + c \cdot 2^2 + \dots \quad (2.1)$$

c	b	a	i
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

In this way, the prescription according to which each state of the network is assigned to the whole number i, is established once for always. If we write this number in binary form we get at once the components of the governed signals - although in the reverse order: ..., c, b, a. The values of the state index i are identical in meaning with the given values of all the components of the governed signals. The state index has therefore the nature of a central parameter, on which all of the other variables of the network depend.

2.1 Transmissibility of Signal Network. A signal conductor between two nodes including the switch which dominates its transmissibility is called a branch of the

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switch signal network. In the case of a relay network we represent a branch as an electrical conductor with two terminals (corresponding to the nodes mentioned) together with a system of relay contacts on which the conductivity of the conductor depends. A system of contacts in the same branch dominating one or several relays is called a relay switch.

The transmissibility of the branch between the nodes M, N is expressed by one of the two statements: "Branch MN is transmissive","Branch MN is nontransmissive". We have therefore only two degrees of transmissibility for the signals. The transmissibility of the branch is given by the transmissibility of its switch. Therefore, its internal characteristics are independent of the relation of the external branches in the network. The transmissibility of the branch is regarded as independent of the network.

In a given working state of the network some of its branches are transmissive and others nontransmissive. A legible picture of the transmissible branches in the given working state of the network is furnished by the partial diagram of the transmissibility of the branches. This is a picture where each of the nodes of the network is depicted by a point and where the joining lines of these points represent the branches through which the signals pass freely (in the given state of the network).

Here each value of the state index i corresponds to one partial diagram of the transmissibility of the branches. The collection of all these partial diagrams constitutes the developed diagram of the transmissibility of the branches.

The transmissibility of the network between the nodes M, N is a concept which we distinguish strictly from the concept of the transmissibility of the branches between the nodes M, N. For ascertaining the transmissibility of the network between the nodes M, N we take into account all possible paths by which the signal can go from M to N (or conversely). In the partial diagram of the transmissibility of the branches we investigate whether for the considered working state

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c	b	a	i
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

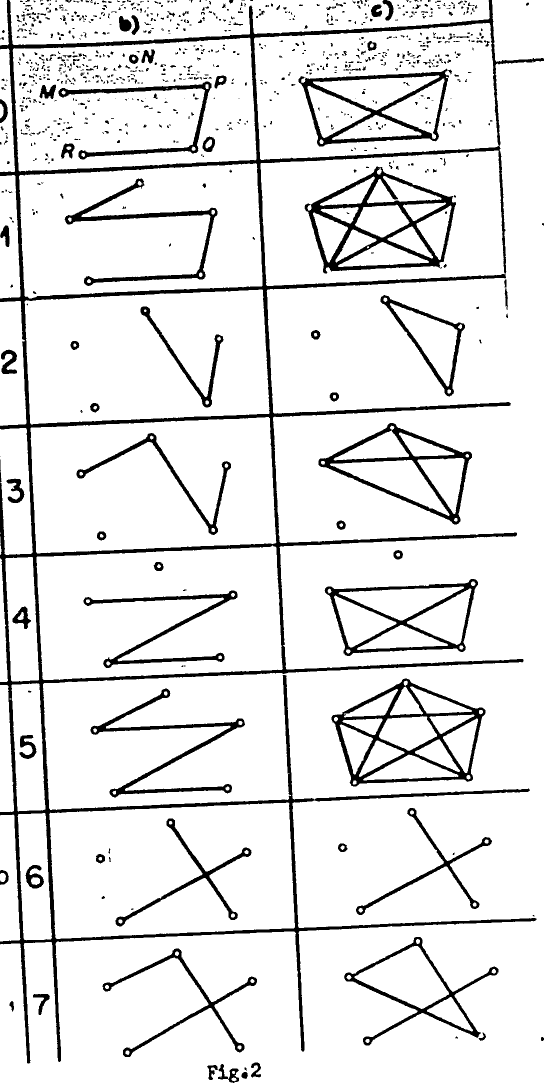

Fig.2

a) Developed diagrams of transmissibility; b) Branches; c) Network

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network the nodes M, N are joined by a line which passes through the one node or the other. If we find such a line we know that the network is transmissive between the nodes M, N.

In the given working state the network is between some of its nodes transmissive and between others nontransmissive. A legible picture of the transmissibility of the network in this working state is furnished by the partial diagram of the transmissibility of the network. This is a picture where each of the nodes of the network is depicted by a point and where the lines directly joining the points show that the network is transmissive between the nodes depicted by these points. A direct joining line is defined here as a line which does not pass through any other node.

Each value of the state diagram index i corresponds to one partial diagram of the transmissibility of the network. The collection of all these partial diagrams, therefore, constitutes the developed diagram of the transmissibility of the network.

Example 8. From the given developed diagrams of the transmissibility of the branches we derive the developed diagram of the transmissibility of the network. The network has eight different working states i = 0, 1, ..., 7. Its signal governor has three components a, b, c. The network has five nodes M, N, P, Q, R, so that $\binom{5}{2} = 10$ branches. The developed diagrams of the transmissibilities are represented in Fig.2. On the left half is the developed diagram of the transmissibility of the branches and on the right half the developed diagram of the transmissibility of the network. The partial diagrams of the transmissibility are arranged in ascending order of the state index i. At each value of the index there is indicated the corresponding value of the signal component.

The working procedure at the drawing of the partial diagrams of the transmissibility of the network will now be explained for the case where i = 0 (i.e., a = b = c = 0). On the corresponding partial diagram of the transmissibility of the branches, the joining lines of the branches MP, PQ, QR, are drawn, which form the

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transmissive signal conductor MPQR. By this signal conductor, the signal passes through between any two of the four joining lines of the nodes M, P, Q, R. The network is therefore transmissive between any two of these nodes. In the partial diagram of the transmissibility of the network (right half of the figure), therefore, we draw the six joining lines MP, MQ, MR, PQ, PR, QR. The quadrangle MPQRM is formed supplemented by every possible diagonal.

In general, it can be said that if in the partial diagram of the transmissibility of the branches we join p-nodes with a single line, we draw in the corresponding partial diagram of the transmissibility of the network the p-square supplemented by every possible diagonal.

In comparing in Fig.2 the case where i = 0 with the case where i = 4, we see that the various partial diagrams of the transmissibility of the branches may correspond with the given partial diagram of the transmissibility of the network.

The partial diagram of the transmissibility of the network is wholly uni-significative with the given corresponding partial diagrams of the transmissibility of the branches. If, however, the partial diagram of the transmissibility of the network contains a three-, four-, or higher p-square supplemented by every possible diagonal, then the given corresponding partial diagram of the transmissibility of the branches is multisignificative (compare i = 5 with i = 1).

2.2 Numerical Symbols of Transmissibility. The transmissibilities between the nodes of the network are denoted by suitable symbols. The symbols of the transmissibility of the networks must, of course, be distinguished from the symbols of the transmissibility of the network. The transmissibility of the branch between the nodes M, N is denoted (MN), the transmissibility of the network between the nodes M, N is denoted MN.

The transmissibility between two nodes in dependence on the working state of the network is expressed by two methods: by algebraic (compare Chapter 3.3) or numerical symbols. In view of the isomorphism discussed in Chapter 1.2, STAT ame

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symbols may be employed in both cases. Here we describe the formation of the numerical symbols of the transmissibility.

The numerical symbol of the transmissibility of the branch (MN) is formed as a suffix to the value of the state index i for which the branch is transmissive between the nodes M, N.

The numerical symbol of the transmissibility of the network MN is formed as a set of the value of the state index i for which it is transmissive between the nodes M, N.

Example 9. Form the numerical symbols of the transmissibility of the network whose diagram of the transmissibility of the branches is given in example 8. Here:

$\|MN\| = \|1\ 3\ 5\ 7\|$	$MN = 1\ 3\ 5\ 7$
$\|MP\| = \|0\ 1\ 4\ 5\|$	$MP = 0\ 1\ 3\ 4\ 5$
$\|MQ\| = \|0\|$	$MQ = 0\ 1\ 3\ 4\ 5\ 7$
$\|MR\| = \|0\|$	$MR = 0\ 1\ 4\ 5$
$\|NP\| = \|0\|$	$NP = 1\ 2\ 3\ 5$
$\|NQ\| = \|2\ 3\ 6\ 7\|$	$NQ = 1\ 2\ 3\ 5\ 6\ 7$
$\|NR\| = \|0\|$	$NR = 1\ 5$
$\|PQ\| = \|0\ 1\ 2\ 3\|$	$PQ = 0\ 1\ 2\ 3\ 4\ 5$
$\|PR\| = \|4\ 5\ 6\ 7\|$	$PR = 0\ 1\ 4\ 5\ 6\ 7$
$\|QR\| = \|0\ 1\ 4\ 5\|$	$QR = 0\ 1\ 4\ 5$

The numerical symbol of the transmissibility of the network MN is formed according to the developed diagram of the transmissibility of the network (right side of Fig.2), at which we write out the value of the state index i of the partial diagram of the transmissibility of the network which has the joining line MN. Here i = = 1, 3, 5, 7.

The numerical symbols of the transmissibility put in the matrixes of the transmissibility of the branches and in the matrixes of the transmissibility of the network are as follows:

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Matrixes of transmissibility of branch:

$$\begin{array}{c|ccc} & M & N & P \\ \hline M & 1 & |MN| & |MP| \\ N & |NM| & 1 & |NP| \\ P & |PM| & |PN| & 1 \end{array}$$

Matrixes of transmissibility of network:

$$\begin{array}{c|ccc} & M & N & P \\ \hline M & 1 & MN & MP \\ N & NM & 1 & NP \\ P & PM & PN & 1 \end{array}$$

A legible picture of the transmissibility of the branch in dependence on the state index is furnished by the diagram of the transmissibility of the branch. This is a picture where each of the nodes is depicted by a point, where the joining lines of the points depict branches, and where at each of the joining lines the numerical symbol of the transmissibility of the corresponding branch is written. The branches without joining lines are permanently nontransmissive.

According to the detailed rules we draw the diagram of the transmissibility of the network. At the joining lines of the nodes we write the corresponding numerical symbols of the transmissibility of the network.

The symbols expressing the transmissibility of the branches are distinguished graphically from the symbols expressing the transmissibility of the network. The existence of both kinds of symbols in the same diagram at the same time is, therefore, permissible. We then speak simply of the diagram of the transmissibility.

Example 10. Draw the diagram of the transmissibility of the network defined in examples 8 and 9. The diagram of the transmissibility is represented in Fig.3.

2.3 Elementary Transmissibility. In the clearest case the branch is always transmissive or always nontransmissive, and we say that there exists elementary transmissibility. However, we also speak of elementary transmissibility in the case where the transmissibility of the branch is changed by the contact of a single relay.

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For the purpose of illustration we shall analyze a concrete case.

In the complex of several networks (Fig.4) assume the branch MN with which the connector of the contact of the relay B is connected by the bus component b of the governed signals a, b, c. The network has eight possible working states, denoted by the values of the state index i = 0, 2, 2, 3, 4, 5, 6, 7. The relations between the values of the signal components a, b, c, and the values of the state index i are given in the accompanying Table.

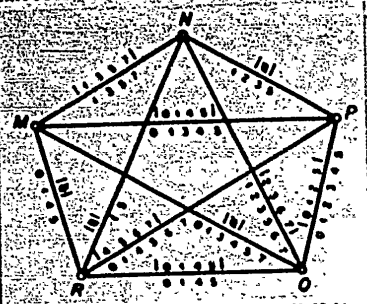
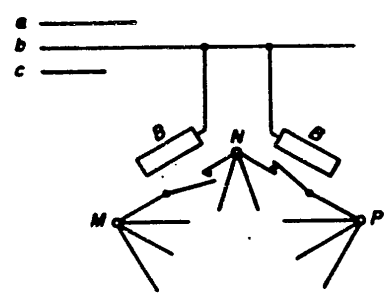


Fig.3 – Diagram of Transmissibility

The branch MN will be transmissive only in the state of the network in which it is transmissively connected by the contact of the relay B, i.e., only when this relay is in the working state. In this case,



c	b	a	i
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Fig.4 – Working States of Network

an exciting impulse enters its winding, and the component b of the governed signal of the network has the value b = 1. The numerical symbol of the transmissibility of the branch MN is composed of the values of the state index i for which b = 1. A glance at the Table shows that the transmissibility of the branch is $|MN| = 2$

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The branch NP will be transmissive only for b = 0. Then the same relay B (it is a matter of indifference whether this relay agress with it, which we have considered above, or whether it is only a relay of the same relay group) is in the resting state, and the disconnector of its contact is transmissive to the signal. In the Table of Fig.4 we find the values of the state index i for which b = 0. By this we determine the numerical symbol of the transmissibility of the branch NP: |NP| = = |0 1 4 5|.

Concerning the branch in which there is the contact of only one relay, we say that it has elementary transmissibility. The numerical symbol of the elementary transmissibility is denoted directly by writing the corresponding signal components according to the following prescription:

For the connector of the contact the elementary transmissibility a (b,c, ...) is given by the numerical symbol derived from the condition a = 1 (b = 1), c = 1,...). With the disconnector of the contact the elementary transmissibility $\bar{a}$ ($\bar{b}$, $\bar{c}$, ...) is given by the numerical symbol derived from the condition a = 0 (b = 0, c = 0, ...).

Example 11. Find the elementary transmissibilities in the network whose signal governor has the five components a, b, c, d, e. Putting in eq.(2;1) the condition a = 1, and for the remaining variables b, c, d, e putting all the combinations of zero and unity, we get the numerical symbols for the elementary transmissibility

$$a = 1\ 3\ 5\ 7\ 9\ 11\ 13\ 15\ 17\ 19\ 21\ 23\ 25\ 27\ 29\ 31$$

Similarly putting a = 0 gives

$$\bar{a} = 0\ 2\ 4\ 6\ 8\ 10\ 12\ 14\ 16\ 18\ 20\ 22\ 24\ 26\ 28\ 30$$

From the analogous formula conditions for b, c, d, e, we get:

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b =	2	3	6	7	10	11	14	15	18	19	22	23	26	27	30	31	
$\bar{b}$ =	0	1	4	5	8	9	12	13	16	17	20	21	24	25	28	29	
c =	4	5	6	7	12	13	14	15	20	21	22	23	28	29	30	31	
$\bar{c}$ =	0	1	2	3	8	9	10	11	16	17	18	19	24	25	26	27	
d =	8	9	10	11	12	13	14	15	24	25	26	27	28	29	30	31	
$\bar{d}$ =	0	1	2	3	4	5	6	7	16	17	18	19	20	21	22	23	
e =	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
$\bar{e}$ =	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Each of the numerical symbols of the elementary transmissibility is composed of 2^{m-1} elements, where m is the number of components of the governed signal network. They therefore contain half of the elements of the fundamental set I composed of all of the values of the state index i.

If we know the numerical symbol of the elementary transmissibility of any m (for example, 5), we can directly derive from it the numerical symbol of the elementary transmissibility for any lower m (for example m = 3). In each of the already-known symbols we simply retain only the elements contained in the fundamental I formed for the lower m. For example, from the symbol given in the last example for m = 5 we derive the symbol for m = 3 by retaining in the original symbol only the elements from 0 to 7.

For the connector of the contact the elementary transmissibility is denoted directly by the letters of the corresponding components of the governed signals. For the contact of the connector these letters are overlined. The following is valid

$$a + \bar{a} \quad b + \bar{b} \quad c + \bar{c} \quad \ldots \quad I. \qquad (2.3;1)$$

In the diagrams of the transmissibility the general symbols a, $\bar{a}$, b, $\bar{b}$, ... may be used wherever the corresponding branch or network has elementary transmissibility.

Example 12. The diagram of transmissibility of the branches and netwo

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alysed in example 9 is represented in Fig.5.

3. Analysis of Relay Networks

By an analysis of the relay network we mean the detailed scheme of its connections and an analysis of its transmissibilities. The nodes in the given network are selected in such a way that all of the branches of the network have elementary transmissibility. The transmissibility of the network can be derived from the developed diagram of the branch transmissibilities. However, we arrive much more quickly at the goal by the method described in this Chapter.

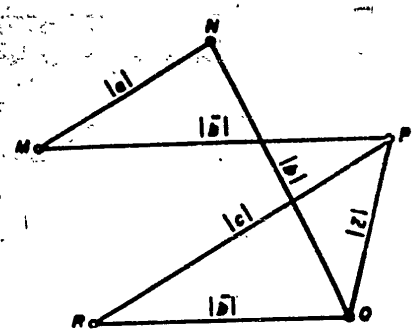

Fig.5 - Diagram of Transmissibility of Branches

3.1 Analysis of Diagram of Transmissibility of Branches. We start with the diagram of the transmissibility of the branches, in which these transmissibilities are expressed by the general symbols $\emptyset$, I, a, $\bar{a}$, b, $\bar{b}$, ... to each branch is assigned the numerical symbol of its elementary transmissibility. Therefore, the numerical symbol of the transmissibility of the network is determined relatively easy.

From the node M we can get to the node N either directly over the branch MN or indirectly over a path composed of other branches. We denote such a path by enumerating the nodes through which it passes. This is a general symbol in the form of MPQ ... STN. The corresponding paths are composed of the branches MP, PQ, ..., ST, TN.

When the numerical symbol of the transmissibility |MP|, |PQ|, ..., |ST|, |TN| of these branches have some element i in common, the network is between the nodes M, N transmissive for this value of the state index. All of the common elements

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of descending order of the numerical symbol of the transmissibility, however, are given of their product (penetration). The total transmissibility along the path MPQ ... STN is therefore

$$|MPQ \ldots STN| = |MP| \cdot |PQ| \cdot \ldots \cdot |ST| \cdot |TN| \qquad (3.1;1)$$

The transmissibility of the network between the nodes M, N is given by the sum (union) of the transmissibilities of all possible such paths from M to N.

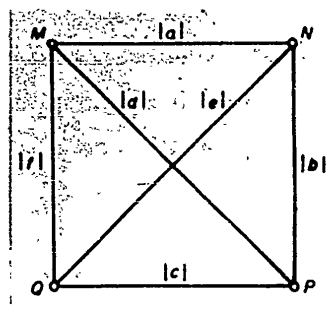

Fig.6 - Diagram of Transmissibility of Branches

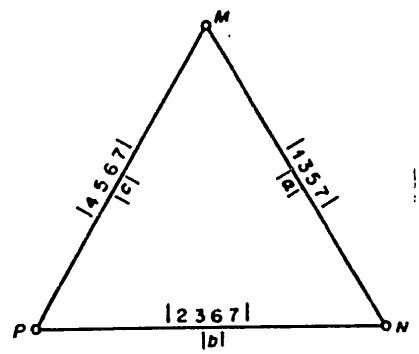

Fig.7 - Diagram of Transmissibility of Branches

Example 13. With the network given in Fig.6, find the transmissibility of the network MN. Use general symbols.

We form the sum (union) of the transmissibilities of all possible paths from M to N. Each of the transmissibilities of this path is formed as the product (penetration) of the numerical symbols of the transmissibilities of the branches connected with each other:

$$|MN| = a + d.b + d.e.c + f.e + f.e.b.$$

This expression has the same form as the Boolian function formed in the u

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way.

Without the adoption of certain expedients for mechanizing the formation of the product of the elementary transmissibilities, the calculation according to eq.(3.1;1) is rather tedious. The transmissibility of the network can be found very conveniently and reliably with the help of the method described below.

Instead of finding the state index for which the network is transmissive over a certain path from M to N, we ascertain whether the network is transmissive between M and N for a certain selected value of the state index. We start at the point M and proceed along the branches whose numerical symbols of the transmissibility contain the selected value of the index. If we succeed in getting to the node N we combine the selected value with the formed symbol of the transmissibility of the network. For the selection we replace in succession all of the elements of the fundamental set I.

Example 14. Carry out the analysis of the transmissibility of the network whose diagram of the transmissibilities of the branches is represented in Fig.7.

For the formation of the numerical symbol of the transmissibility of the network between the nodes M, N we select in succession i = 0, 1, 2, ..., 7, and for each value separately we try to proceed in the network from M to N.

For i = 0 there is no path

= 1 there is the path MN

= 2 there is no path

= 3 there is the path MN

= 4 there is no path

= 5 there is the path MN

= 6there is the path MPN

= 7 there is the path MN

Transmissibility of network:
MN = 1 3 5 6 7

Similarly we establish the remaining transmissibilities of the network:

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NP = 2 3 5 6 7

PM = 3 4 5 6 7

3.2 Numerical Bones. For analyzing the relay network, we start with the diagram of the transmissibilities of the branches composed exclusively of the elementary transmissibility. There are several different ones, their numerical symbols are given once for always. For this purpose we prepare long paper strips (Fig.8),

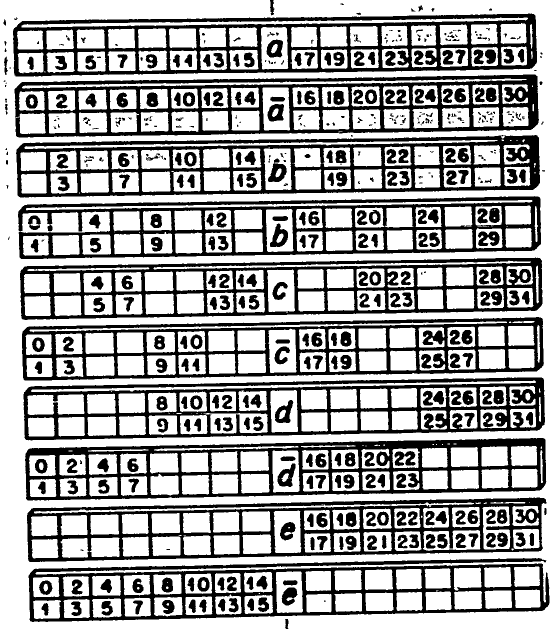

Fig.8 - Numerical Bones

and each of them is provided with several numerical symbols of the elementary transmissibilities together with the corresponding general symbol. Of such numerical bones a, $\bar{a}$, b, $\bar{b}$, ... a sufficient number is prepared.

For analyzing the given relay network, we compose of the numerical bones a model of the diagram of the transmissibilities of the branches. Therefore,

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the relay contacts connected with the network corresponds in the model to one bone.

Then we determine the transmissibility of the network in the manner described in the text and represented in Fig.7. The bones may be regarded as a species of filter which along their length are permeable only to the index denoted on them.

The bones are an advantageous expedient not only for analyzing the given network but also for its synthesis. They are easily shifted, and enable rapid changes in the diagram during its synthesis. With them the transmissibility of the network is determined with great reliability.

The bones formed for the signal governor, consisting, for example, of five components, are suitable for the solution of the problem also when the components of the signal governor have to be changed.

3.3 Analysis of Numerical Symbols. The diagram of the transmissibilities of the branches of the given network contains exclusively the elementary transmissibilities. At the synthesis of the network, however, we have to do with diagrams where the transmissibilities of the branches are expressed by symbols which are not elementary. This means that the transmissibility of none of the branches can be changed by the contact of one relay. We therefore introduce the term relay switch as a device which forms a component of the branch and dominates its transmissibility with the contact of one or several relays. If the contact of only one relay is in the branch, this is only a special case of the relay switch. We often call it the switch element, and say that it has the elementary transmissibility.

The nonelementary symbol of the transmissibility f of a branch represents the dependence of the transmissibility of the branch on the state index of the network. However, we have scarcely anything to say about the connections of the contacts of the relays by which the transmissibility f can be obtained. The numerical symbol f is transformed because in the algebraic expression, either the sum (union) of the products (penetrations) or the product (penetration) of the sums (unions) of the signal components (elementary transmissibilities) a, $\bar{a}$, b, $\bar{b}$, ... is formed. We

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obtain this only from the fundamental expressions:

$$f = \sum (\dot{a}\dot{b}\ldots) \qquad (3.3;1)$$

$$f = \prod (\dot{a} + \dot{b} + \dot{c}\ldots) \qquad (3.3;2)$$

where the dots above the symbols mean that the corresponding product of the sums (or sum of the products) of the corresponding variables is either wholly absent or contains it unsupplemented or in the supplement.

An example of the form just described is the expression

$$f = a + b\bar{c} + \bar{b}d = (a + b + d)(a + \bar{b} + \bar{c}) \qquad (3.3;3)$$

The importance of the transformation of the functions given by the numerical symbols in the described fundamental form can be seen from the large number of forming methods given in Bibl.3. We use principally the method of tabulation.

The algebraic expressions obtained by transformation of the numerical symbols are isomorphous (same form) with the expressions of Boolian algebra, and can be used in a large majority of the words. The variables a, b, c, ... therefore acquire one of two permissible values: 0, 1. These values describe the state of the corresponding relay groups A, B, C, ... according to definition: the value zero corresponds to the resting state, the value 1 corresponds to the working state.

The algebraic expression by which we express a transmissibility in the network has therefore for us two meanings simultaneously: On the one hand it prescribes how by union and penetration of the numerical symbols of the transmissibility there is obtained the numerical symbol of the transmissibility, and, on the other hand, it is the algebraic expression of the Boolian functions at which the values 0, 1 of the variables a, b, c, ..., can be obtained, and, by addition (Boolian) or multiplication, their functional value calculated (0 denotes nontransmissibility, 1 denotes transmissibility).

To this work a Table of products (penetrations) of the form abcde is annexed;

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according to this Table (page 196) we carry out the analysis of the numerical symbols for m = 5. We find that all of the tabulated elements in this series are contained in some of the given numerical symbols f corresponding to the product $\bar{a}\bar{b}\bar{c}\bar{d}$ of the components of the sum in eq.(3.3;1). The Table was prepared by Z.Korvas in such a way as to make the finding of the components as convenient as possible.

Example 15. Algebraize the given numerical symbol s. Use the Table. Arrange in the form of the Table

# =	1	2	4	5	6	9	10	11	13	15		
	1			5		9			13		.....	$+\ a\ b$
		2			6						.....	$\bar{a}\ b\ \bar{d}$
		2					10				.....	$+\ \bar{a}\ b\ \bar{c}$
			4	5							.....	$\bar{b}\ c\ \bar{d}$
			4		6						.....	$+\ \bar{a}\ c\ \bar{d}$
						9		11	13	15	.....	$+\ a\ d$
							10	11			.....	$b\ \bar{c}\ d$

First of all it should be noted that $i \leq 15$, i.e., that the example concerns a circuit with four variables a, b, c, d. Accordingly we disregard in the Table the values above 15 and omit the variable e in all of the expression.

The Table begins with the symbols containing zero. Since the given symbol s does not contain zero, we proceed at once to the part of the Table where the numerical symbols begin with unity. Here we find the numerical symbol all of whose elements are contained in the given numerical symbol. Such a symbol is 1 5 9 13 = $a\bar{b}$. The symbol found is written according to the above equation. We then proceed further in the same part of the Table and seed the further satisfying symbols which, however, are not completely contained in any of the symbols which we have already taken from the Table. For this reason, for example, the symbol 1 5 = $a\bar{b}\bar{d}$, does not satisfy us, because it is completely contained in the symbol 1 5 9 13 [compare with eq.(1.1;14)]. We find that no other symbol beginning with unity is satisfying. In the part of the symbols beginning with two, two symbols satisfy: 2 6 = $\bar{a}b\bar{d}$, 2 10 = $\bar{a}b\bar{c}$. It is unimportant that they contain indexes in common. It STAT portant

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that the second is not fully contained in the first. Next we proceed directly to the part of the symbols beginning with index 4. We proceed further in the same way through the whole Table. The product which we take represents the components of the function s, i.e., the following is valid

$$s = a\bar{b} + \bar{a}b\bar{d} + \bar{a}b\bar{c} + \bar{b}c\bar{d} + \bar{a}c\bar{d} + ad + b\bar{c}d. \qquad (3.3;4)$$

The fact that the expression is correct can be seen at once; by union of the sets written under the algebraized symbols, the given symbol is actually formed. Examining more closely, we see that some of the selected components are necessary while others can replace each other. Thus the index 1 is formed solely by the term $a\bar{b}$. For this reason this component is essential, and cannot be replaced with any other. We denote by the plus sign. For a similar reason the component ad (forming 15) is essential. To the essential components we further add the least terms. We assume that the component $\bar{a}b\bar{c}$ is a remainder of the component $b\bar{c}d$, and that $\bar{a}c\bar{d}$ is a remainder of the components $\bar{a}b\bar{d}$, $\bar{b}c\bar{d}$. The function s is therefore given by the shortest sum of the products:

$$s = a\bar{b} + \bar{a}d + \bar{a}b\bar{c} + \bar{a}c\bar{d} \qquad (3.3;5)$$

If we want to express the same numerical symbol s in the form of the product of the sums (3.3;2) we start with the supplement $\bar{s}$ and carry out its analysis with the help of the Table. We transform the result into the supplement according to example 5, and get the definitive expression in the required form.

$$\begin{array}{llll}
\bar{s} \equiv 0\ 3\ 7\ 8\ 12\ 14 & & & \\
\quad 0 \quad\ \ 8 & \ldots\ldots & + & \bar{a}\,\bar{b}\,\bar{c} \\
\quad\ \ 3\ 7 & \ldots\ldots & + & a\,b\,\bar{d} \\
\quad\quad\ \ 8\ 12 & \ldots\ldots & & \bar{a}\,\bar{b}\,d \\
\quad\quad\quad\ \ 12\ 14 & \ldots\ldots & + & \bar{a}\,c\,d
\end{array}$$

Therefore, $\bar{s} = \overline{abc} + ab\bar{d} + \bar{a}cd$. We get the supplement:

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$$x = (a + b + c)(\bar{a} + b + d)(a + c + d) \qquad (3.3;6)$$

Equations (3.3;5) and (3.3;6) express the same function in the two fundamental forms.

4. Synthesis of Relay Networks

The problems solved in this work are not of the most general type. We are interested in concentrating on individual circuits where we assume that the components of the governed signals a, b, c, ... act simultaneously and bring the network to the resultant working state.

In this work we are also uninterested in problems where the transmissibility expressed by Boolian and numerical symbols satisfies the condition entering into the relation of internal symmetry which can be utilized for solving the problem. An important example of such a problem is the synthesis by addition of any number of binary coded numbers.

4.1 Statement of Problem of Synthesis of Network. In this work we concentrate on the solution of the following fundamental problem:

On the relay network the following information is given:

1. The signal governor has m components a, b, c, ...

2. The transmissibilities between the main nodes M, N, P, ... are prescribed as the function of the state index i.

Determine the transmissibilities of the branches in such a way as to satisfy the prescribed transmissibility of the network.

The main nodes are those between which the transmissibilities are prescribed by the problem. The remaining nodes are called subsidiary or auxiliary.

The transmissibility of the network is given by the Table. In this work we express it by either the numerical symbol or the corresponding algebraic expression.

The network may have 2^m possible states. However, the problem need not pre-

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scribe the transmissibility for each of these states. The range of variability of the state index i is therefore limited to a certain subset of the fundamental set I.

If p-main nodes are given, the maximal transmissibility that can be prescribed in the problem is $\binom{p}{2}$.

4.2 Criterion of Solvability. For the problem of the synthesis of a relay network to be solvable the transmissibility of the network must be prescribed which satisfies the condition which we call the condition of consistence of the transmissibility of the network. This condition is the most conveniently represented by the developed diagram of the prescribed transmissibility of the network. We assume first of all that the problem prescribes the transmissibility for each of the pairs of main nodes.

The condition of consistence of the transmissibility of the network is defined as follows: the prescribed transmissibility of the network is consistent if the developed diagram of the transmissibility of the network contains exclusively closed polygons of which each has all of the diagonals.

Example 16. In the triangular network M, N, P the transmissibilities are prescribed.

MN = 0 1 2 5

NP = 0 1 3 7

PM = 1 4 6 7

The problem thus stated is insolvable because in the state i = 0, 7 the condition of consistence of the transmissibilities of the network is not fulfilled. Since for i = 0 the network is transmissive between the nodes M, N and between the nodes N, P it must also be transmissive between the nodes P, M. The corresponding partial diagrams of the transmissibility of the network must contain a triangle. By analogy it can be said that the network must be transmissive between the nodes M, N for i = 7.

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4.3 Supplementary Given Matrixes of Transmissibility of Network. In the problem of the synthesis of a network, the transmissibilities of all of the pairs of main nodes are not prescribed. Therefore, some of the elements of the matrixes of the transmissibility of the network are not prescribed.

For example, for a network with three main nodes M, N, P, the transmissibilities MN, MP are often prescribed, while the transmissibility NP is not prescribed*.

One of the partial problems of our working procedure is the maximal supplementation of the matrixes of the transmissibility of the network **. Between the one pair of nodes for which the transmissibility of the network has not been prescribed, we assume provisionally transmissibility for the largest possible number of states of the network provided the transmissibility prescribed for the other pair of nodes is left undisturbed.

We must explain here more fully the terms "prescribed transmissibility" and "permissible transmissibility".

The Prescribed Transmissibility of the Network between the nodes M, N represents the functional conditions which must be fulfilled by the network being formed. The prescription is given which must be coordinated with the transmissibility MN for every permissible state of the network.

The Permissible Transmissibility of the Network between the nodes P, Q is given by enumerating the states of the network, at which we taken any transmissibility between the nodes P, Q without influence on any of the prescribed transmissibilities of the network.

---

* In the literature relay networks are often mentioned with one input (M) and two outputs (N, P). With our method the number of inputs and outputs is a matter of indifference, so that we can simply ignore it altogether. We regard it as one of the suitable methods.

** The importance of the supplementary problems is discussed in the seminary work of M. Valach, proposed decoder.

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From this definition it follows at once that the nodes P, Q cannot be nodes between which the transmissibility is definitely prescribed.

Consider two problems A, B, which are exactly the same except for the permissible transmissibility between the nodes P, Q. Let problem A be stricter than problem B, i.e., let every transmissibility which is permissible in problem A be also permissible in problem B, but not conversely. Then all solutions of problem A are solutions of problem B, but solutions of problem B may exist which are not solutions of problem A. Therefore, the number of solutions of problem B cannot be smaller than the number of solutions of problem A.

Incomplete data of the matrixes of the transmissibility of the network prescribe the transmissibility only between some of the pairs of main nodes. Between the remaining pairs at this prescription, of course, transmissibility follows from the condition of consistence of the transmissibilities. In the sense of our definition, of course, these are not permissible transmissibilities. On the basis of what has been stated above, if follows that the number of possible solutions of the problem is not decreased if we assume permissible transmissibility for all of the pairs of nodes where the transmissibility is not definitely prescribed. On the other hand, it can be shown that the number of possible solutions is much greater here, and that some of these solutions are much simpler than any of the solutions of the stricter problem. An example will be given later.

The permissible transmissibility of the network is clearly determined as follows. We draw the developed diagram of the prescribed transmissibility of the network. In it we draw for each i the partial diagram, in which light joining lines indicate the pairs of nodes between which the problem prescribes nontransmissibility of the network and heavy joining lines indicate the pairs of nodes between which the problem prescribes transmissibility. In each of the partial diagrams, therefore, we draw

1. The transmissibility following from the condition of consistence of the

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transmissibilities of the network (heavy geometrical picture supplemented with heavy joining lines on closed polygon supplemented with diagonals).

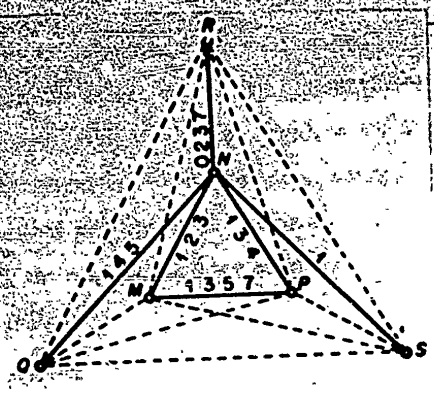

Fig.9 - Diagram of Prescribed Transmissibilities of Network

2. The permissible transmissibilities (in the greatest possible number) in heavy lines drawn across the picture, in such a way that none of them coincides with a light joining line but in such a way that the formed picture is a closed polygon supplemented with diagonals.

The method is more fully explained by the following example.

Example 17. In the problem of a network which has three independent variables a, b, c the transmissibilities of the network are prescribed by the following matrixes:

	M	N	P	Q	R	S
M	1	1 2 3	1 3 5 7			
N		1	1 3 4	1 4 5	0 2 3 7	1
P			1			
Q				1		
R					1	
S						1

The diagram (undeveloped) of the prescribed transmissibilities of the network is represented in Fig.9.

The permissible transmissibilities of the network are best determined on the developed diagrams of the transmissibilities of the network - Fig.10. It should be noted that for some values of i the problem is ambiguous. Thus, for example, for i = 0 it is possible to permit transmissibility for the triangle MQS or for the

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triangle PQS. Ambiguity is also present at i = 6. The reader is advised to analyse in fairly great detail the diagram of i = 5.

If it were desired to find every possible solution of the given problem, it would be necessary to continue the work on the basis of every possibility. In practice we usually select one of the possibilities (as indicated by the requirements of the particular case), and formulate the whole network. If we are not satisfied with the result we turn to another variant of the permissible transmissibility, and formulate another network according to it.

Finally, the maximal matrixes of the transmissibility of the network in our case are as follows:

	M	N	P	Q	R	S
M	1	1 2 3	1 3 5 7	0 1 6 7	2 3 4 5 6	0 1 4 5 6 7
N		1	1 3 4	1 4 5	0 2 3 7	1
P			1	1 2 4 7	3 5	1 2 5 7
Q				1	6	0 1 2 3 6 7
R					1	4 5 6
S						1

4.4 Selection of Transmissibilities of Branches. A diagram which is supplemented with the greatest possible number of permissible transmissibilities of the network is called the maximal diagram of the transmissibility of the network. In it the joining lines of the nodes are denoted by the corresponding numerical symbols of the transmissibilities of the network. The pairs of nodes between which the transmissibility is fully prescribed are joined by a solid line and the remaining pairs of nodes by a broken line.

The maximal diagram of the transmissibilities is algebraized, i.e., we replaced the numerical symbols of the transmissibilities of the network with the algebraic expressions in the form of eq.(3.3;1). To the partial product of these expressions we usually assign the corresponding partial numerical symbol.

Each of the algebraic expressions expressing the transmissibility between a pair of nodes (i.e., the prescribed or also the permissible transmissibility) also

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expresses the structure of the serioparallel connections of the branches of the relay switch, whose elementary synthesis has already been described in several

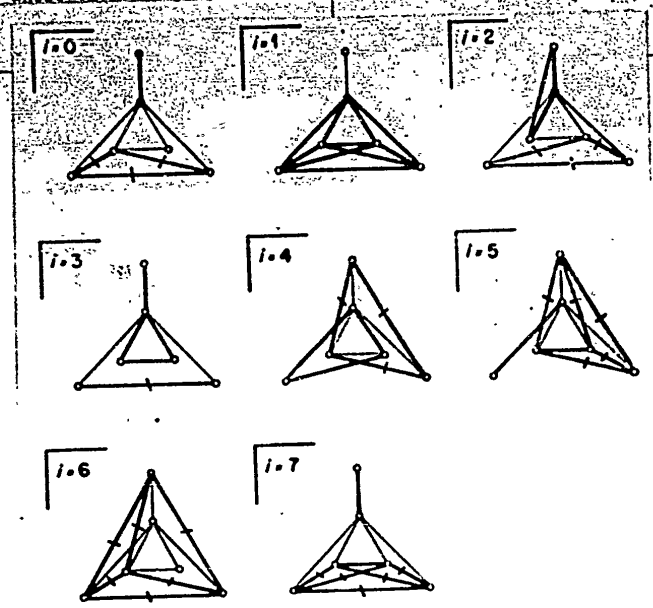

Fig.10 - Developed Diagrams of Transmissibility of Network

places*. When a relay switch formed in this way connects between the corresponding nodes of the network, one of the correct solutions of the given problem is obtained. This solution would be the most uneconomical utilization of the whole network (the developed diagram of the transmissibility of the branches would agree with the developed diagram of the transmissibility of the network).

We have already described the fundamental branch, according to which we shall now discuss a simple example.

Example 18. We have to carry out the synthesis of a network with three signal

* We assume that the reader is familiar with certain fundamental works in this field. We recommend M.A.Gavrilov, Theory of Relay Contact Scheme, Czech translation (3).

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components a, b, c, for which the following transmissibilities of the network are prescribed:

$$MN = 1\ 5\ 6$$

$$MP = 1\ 6\ 7$$

The developed diagrams of the transmissibility of the network are represented in Fig.11. The denotations are according to Fig.12.

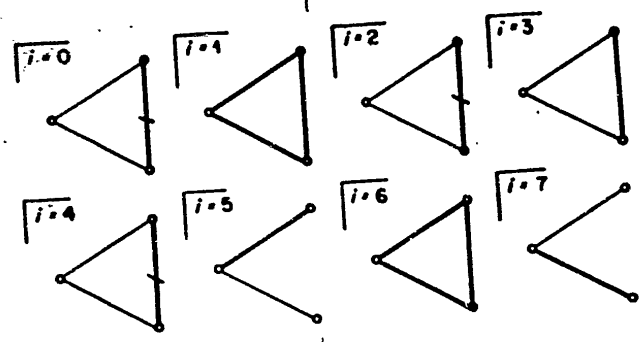

Fig.11 - Developed Diagrams of Transmissibility of Network

We see that the problem prescribes between the nodes P, N the transmissibilities only for i = 1, 6 (indicated by the solid lines). However, transmissibilities are also permissible in the states i = 0, 2, 3, 4 (denoted by the broken line). The transmissibilities concerned in the solution of the problem are:

$$NP = 0\ 1\ 2\ 3\ 4\ 6$$

The transmissibilities of the network are algebraized with the help of the Table. For this we take only the indices i = 0, 1, ..., 7. We get:

$$MN = 1\ 5\ 6 \qquad 1\ 5 = +ab \qquad 6 = +\bar{a}bc$$

$$MP = 1\ 6\ 7 \qquad 1 = +a\bar{b}\bar{c} \qquad 6\ 7 = +bc$$

$$NP = 0\ 1\ 2\ 3\ 4\ 6 \qquad 0\ 1\ 2\ 3 = +\bar{c} \qquad 0\ 2\ 4\ 6 = +\bar{a}$$

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The algebraized maximal diagram of the transmissibility of the network is represented in Fig.12.

It should be noted that 1 is the penetration of the numerical symbols 1 5 and 0 1 2 3. This means that if we select the transmissibility of the branch $|PN| = |\bar{c}|$ and the transmissibility of the network $|MN| = |a\bar{b}|$, then for i = 1, the network, due to the transmissibility of the path MNP, will be transmissive between the nodes M, P, so that it is superfluous to give the branch MP the transmissibility $|\overline{abc}| = 1$. If the above-mentioned transmissibility is not selected in the branch PN, then the branch MP must be given the transmissibility $\overline{abc}$.

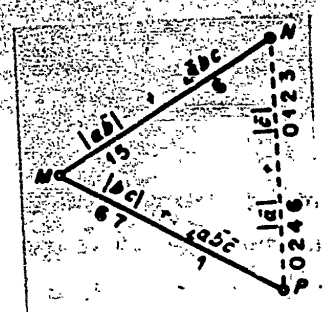

Fig.12 - Algebraized Maximal Diagram of Transmissibility of Network

The selected transmissibilities of the branches are indicated on both sides

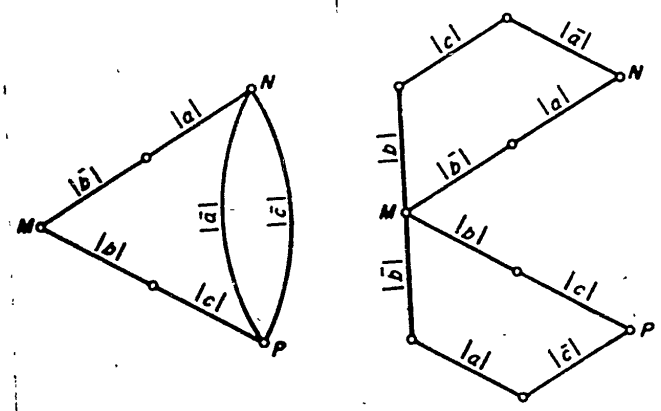

Fig.13 - Diagrams of Transmissibilities of Branches

by diagonals, which are traced according to the symbols of the transmissibility of the network which satisfy our selections. In our case, we indicate by the diagon-

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als $|ab|$, $|\bar{c}|$, and trace $\bar{abc}$. Similarly, we indicate by $|bc|$, $|\bar{a}|$ and trance $\bar{abc}$.

For the selection of the transmissibilities of the branches we try to satisfy the specified transmissibilities of the network, at which we use the permissible transmissibilities only as a convenient expedient. We continue with the selection of the transmissibilities until all of the components of the prescribed transmissibilities of the network are between diagonals or are traced.

In Fig.13 we see on the left the diagram of the transmissibilities of the branches when the greatest transmissibility is permitted between the points N, P. On the right is the diagram corresponding to the stricter problem, where the branch NP is nontransmissive.

At closer inspection of these diagrams we see that the inclusion of the permissible transmissibilities considerably simplifies the solution of the problem.

The algebraic expressions are unavoidable for the selection of the transmissibilities of the branches because it is the picture of the structure of the relay switch which we wish to simplify. However, they are not the most suitable from the viewpoint of the relations according to which we select the transmissibilities. In the work on the numerical symbols we refrained from the application of many of the statements of Boolian algebra, whose applicability was not always directly clear. For this reason the explanation of the fundamental branch for the selection of the transmissibilities of the branches is best carried out directly with the help of the numerical symbols.

4.5 Fundamental Rules for Selection of Transmissibility of Branches. The selection of the transmissibilities of the branches is carried out on the algebraized maximal diagram of the transmissibilities of the network. Since the formation of this diagram was not unambiguous, the working procedure for the selection of the transmissibilities is also not unambiguous. The number of variants is sometimes so great that we must be satisfied with a result which does not come anywhere near the ideal.

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We base the selection of the transmissibility on two fundamental rules.

Rule 1. Given that in the diagram of the transmissibilities of the network there is a closed path PQR ... SP, at which the penetration of the corresponding numericals is p. Given that between the two neighboring nodes P, Q, this circuit is a component of the transmissibility of the network x = $\bar{a}\bar{b}c$ .... Let this component be contained in p, i.e., let the following be valid x + p = p. We select the transmissibility |QR|, ..., |SP| of the branch of the path QR, ..., SP in such a way that x is contained in its penetration q, i.e., that x + q = q satisfies the component x of the transmissibility of the network between the nodes P, Q.

Example 19. Carry out the selection of the transmissibilities of the branches given by the diagram of the transmissibilities of the network (Fig.14). The penetrations of the symbols of the transmissibilities in the circuit MNPM are p = 0 4 6. Therefore, it is possible to satisfy any of the following network transmissibilities: $\overline{ab}$ = 0 4 or $\bar{a}bc$ = 6 or $\bar{a}c$ = 4 6. The component $\overline{bc}$ = 0 1 is not contained in the penetration. Since there is not present here any other closed path in which the penetration of the transmissibilities is contained we must select it as the component of the transmissibility of the branch PN. The selection is denoted by a vertical traverse, which gives the symbol denoting the transmissibility of the branch.

The most complicated algebraic expression of the network is $\bar{a}bc$ = 6. This is an indication against its selection as a component of the transmissibility of the network. Therefore we select in the circuit MNP in the branches the transmissibilities $\bar{a}$, $\bar{a}c$, and trace $\bar{a}bc$. However, the penetration of all of the selected transmissibilities of the path MNP is q' = 0 4 6. Therefore, the components of the transmissibilities of the network given by the product $\overline{ab}$ = 0 4 are also satisfactory (so that we include it).

Remark: We think that the problem confirms the suitability of the numerical symbols for this kind of problem.

Rule 2. Given in the diagram of the transmissibilities of the network the

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triangular circuit MNPM. Assume that we select in its branches the following components of the transmissibility:

$$|MN| = f, \quad |NP| = g, \quad |PM| = h.$$

Assume further that for the selected components the following is valid

$$| f + g + h = f + g. \qquad (4.5;1)$$

i.e., that f + g contains h. Further, let the branches of the triangle contain the network transmissibilities x, y, z ..., each of which is contained in the transmissibility h, i.e., assume that the following is valid

$$x + h \quad y + h \quad z + h \quad \ldots \quad h \qquad (4.5;2)$$

Thus all of the components x, y, z ... are satisfactory belonging to the various branches of the triangle.

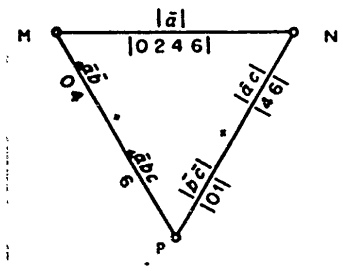

Fig.14 - Selection of Transmissibilities of Branches According to Rule 1

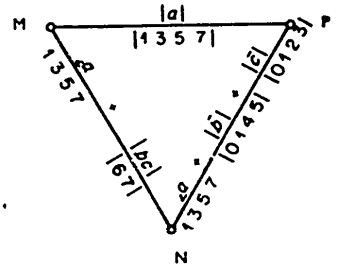

Fig.15 - Selection of Transmissibilities of Branches According to Rule 2

The proof of this rule is simple. Since eq.(4.5;1) is valid every state index i provided with the symbol h is present in the symbol f or in the symbol g. Physically this means that if the branch PM is transmissive then, the branch MN or the branch NP (or, finally, both branches) is also at the same time transmissive. But

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then the network is transmissive between all three pairs of nodes for every state index contained in the symbol h. According to eq.(4.5;2), however, the state index of the components of the network transmissibilities x, y, z ... is contained in the symbol h. The transmissibility given by this symbol is therefore satisfactory (we may trace it).

Example 20. Carry out the selection of the transmissibilities of the branches given by the diagram of the transmissibilities of the network (Fig.15). We select $f = |MN| = bc$, $g = |NP| = \bar{b} + \bar{c}$, $h = |PM| = a$ where eq.(4.5;1) is valid as a result of the relation $|MN| + |NP| = f + g = I$. For the components of the transmissibilities of the network $MN = a = x$, $NP = a = y$, it is clear that eq.(4.5;2) is valid. This proves that the above selection gives the network transmissibilities in the sides MN and NP (we may trace them).

Remark: The application is rule 2 is simpler than the application of rule 1. Unfortunately, rule 2 is not applicable as frequently as rule 1.

Remark: Rule 2 can be solved for quad-rangles.

4.6 Example of Synthesis of Network. We present an example with which the connections between all of the steps described so far can be seen.

Carry out the synthesis of a relay network which is governed by the governor of the signals a, b, c, d, e, and which form the output signals x, y, z, u given by the Table of the usual form. The signals a, b, c, d, e with the digits t = = 0, 1, ..., 9 in the code of the Powers machine for perforated cards are transformed into the signals x, y, z, u in the double code. The signal components x, y, z, u form the relay network. Instead of the components of the signal branches separately we compose the network with which the network transmissibilities are suitably prescribed. The fundamental scheme given in Fig.16 is better for our purpose. It is sufficient to prescribe the transmissibilities of the network between the main nodes M, N, P, Q, R in such a way that

$$MN = x, \quad MP = y, \quad MQ = z, \quad MR = u \qquad (4.6;1)$$

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The problem is incomplete in two senses. First, all of the transmissibilities of the network are not prescribed, and second, the transmissibilities of the network for all of its possible states are not prescribed. With regard to the definition of the state index i according to eq.(2;1), the fundamental set I has only 10 different elements:

$$I = 0\ 1\ 2\ 3\ 4\ 5\ 8\ 9\ 16\ 17 \qquad (4.6;2)$$

The numerical symbols of the transmissibilities of the network therefore contain exclusively only this index. According to the given Table:

i	e d c b a	i	u z y x
0	0 0 0 0 0	0	0 0 0 0
16	1 0 0 0 0	1	0 0 0 1
17	1 0 0 0 1	2	0 0 1 0
8	0 1 0 0 0	3	0 0 1 1
9	0 1 0 0 1	4	0 1 0 0
4	0 0 1 0 0	5	0 1 0 1
5	0 0 1 0 1	6	0 1 1 0
2	0 0 0 1 0	7	0 1 1 1
3	0 0 0 1 1	8	1 0 0 0
1	0 0 0 0 1	9	1 0 0 1

$x = MN = 1\ 2\ 4\ 8\ 16$

$y = MP = 2\ 5\ 8\ 17$

$z = MQ = 2\ 4\ 5\ 9$

$u = MR = 1\ 3$

Figure 17 represents the diagram of the prescribed transmissibilities with which we start the supplementation of the given problem. In Fig.18 the corresponding developed diagram of the transmissibilities of the network is represented. For its formation we proceed as follows:

1) By light joining lines in the partial diagrams the pairs of nodes are indicated which are to be nontransmissive according to the specifications;

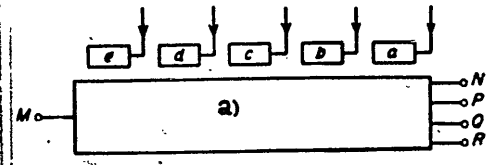

Fig.16

a) Relay network

2) By heavy joining lines the pairs of nodes are indicated which are to be

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transmissive according to the specifications.

The supplemented diagram of the prescribed transmissibilities is constructed as follows:

3) We trace the transmissibilities following from the condition of consistence of the transmissibilities (we supplement the heavy picture to a closed polygon with supplementary diagonals);

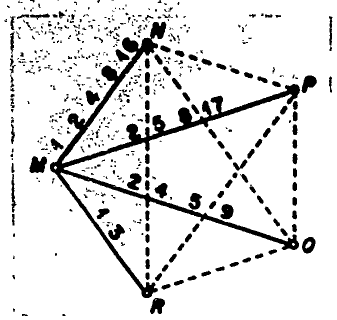

Fig.17 - Diagram of Prescribed Transmissibilities of Network

4) We add the largest possible number of permissible transmissibilities. These transmissibilities are drawn in heavy joining lines (superposed traverses), at which we observe two rules: each picture formed in this way must be a polygon supplemented with diagonals, and no side of this polygon dare coincide with a light joining line, where transmissibility is prohibited.

In Fig.18 the transmissibilities of the network have been supplemented with 22 joining lines in all. The problem of the supplementation of the transmissibilities of the network is then expressed by the following matrixes:

	M	N	P	Q	R
M	1	1 2 4 8 16	2 5 8 17	2 4 5 9	1 3
N		1	0 2 3 8 9	0 2 3 4 17	0 1 5 9 17
P			1	0 1 2 3 5 16	0 4 9 16
Q				1	0 8 16 17
R					1

The matrixes are symmetrical, so that the symbols are not written below the diagonals. The symbols of the transmissibilities are algebraized according to the Table. Since the fundamental set I has only 10 elements given in eq.(4.6;2) we take in the Table only these indices. We take a piece of paper on whose upper edge we denote with check marks the only columns in the Table in which we are interested.

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We then run down the Table and stop only at the check marks. In this way the components of the algebraic expressions are found more quickly.

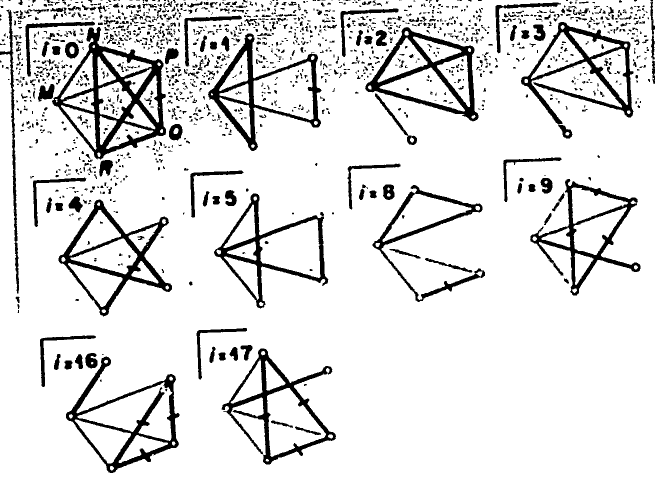

Fig.18 – Developed Diagrams of Transmissibilities of Network

The working procedure is shown in detail in Fig.19. Let us analyze more fully the numerical symbol MN = 1 2 4 8 16. Since 0 is not in the symbol but is in the fundamental set I, all of the symbols with zero in the Table are skilled (0 is not permitted in the symbol). Of the numerical symbols beginning with unity only 1 = $\bar{a}\bar{b}\bar{c}\bar{d}\bar{e}$ is satisfactory. Of the numerical symbols beginning with 2 the symbol 2 6 10 14 18 22 26 30 = $\bar{a}b$ is satisfactory, because according to the check mark at the upper edge of our paper guide we notice that 2 is contained in the fundamental set I, and the symbol 2 is a part of the symbol MN. All of the other satisfactory symbols beginning with 2 are contained in the symbols which we have already selected. The group beginning with the digit 3 in the Table are skipped. In the group of symbols beginning with the digit 4, the symbol 4 6 12 14 20 22 28 30 = $\bar{a}c$ is satisfactory. Of it only 4 is valid. We skip the next group beginning with the number 5, but dare not skip the groups beginning with 6, 7, because while these two numbers

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are not elements of the fundamental set I they may nevertheless appear in symbols which are satisfactory. In these two groups of symbols there are, of course, symbols which are permissible, but none of them contains any new components of the number symbol MN. Of the group of symbols beginning with the number 8, 10 12 14 24 26 28 30 = $\bar{a}d$. We skip the group of symbols beginning with the number 9, but run through

MN = 1 2 4 8 16		MP = 2 5 8 17	
1	$abc\bar{d}\bar{e}$	2	$\bar{a}b$
2	$\bar{a}b$	5	ac
4	$\bar{a}c$	8	$\bar{a}d$
8	$\bar{a}d$	17	ae
16	$\bar{a}e$		
MQ = 2 4 5 9		MR = 1 3	
2	$\bar{a}b$	1 3	$a\bar{c}\bar{d}\bar{e}$
4 5	c		
9	ad		
NP 0 2 3 8 9		NQ = 0 2 3 4 17	
0 2 8	$\bar{a}\bar{c}\bar{e}$	0 2 4	$\bar{a}d\bar{e}$
2 3	b	2 3	b
8 9	d	17	ae
NR 0 1 5 9 17		PQ = 0 1 2 3 5 16	
0 1	$bcd\bar{e}$	0 1 2 3	$c\bar{d}\bar{e}$
1 5 9 17	ab	0 2	16 + $ac\bar{d}$
		1 3 5	+ ade
		2 3	+ b
PR 0 4 9 16		QR 0 8 16 17	
0 4 16	abd	0 8 16	$ab\bar{c}$
9	ad	16 17	e

Fig.19 - Algebraization of Numerical Symbols for

I = 0 1 2 3 4 5 8 9 16 17

the groups having as the initial number 10, 11, 12, 13, 14, 15. If none of the symbols in these parts of the Table contain further symbols of the transmissibility MN we proceed to the part with the initial number 16. Here we find the symbol 16 18 20 22 24 26 28 30 = $\bar{a}e$ of which we use only the 16. This completes the analysis of

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numerical symbols.

Remark: At the analysis of the transmissibilities of the network PQ we found that the sum of three products denoted + is sufficient. There is, however, no objection to using all four products. At the later reduction, the correct application

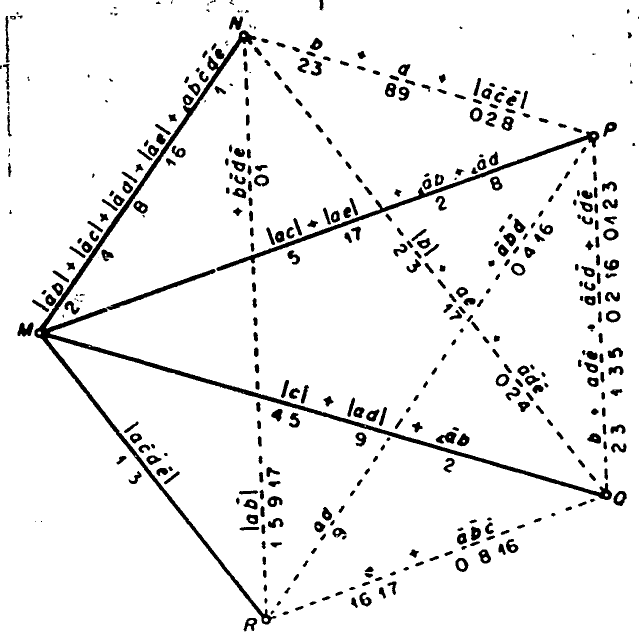

Fig.20 - Selection of Transmissibilities of Branches

of rules 1 and 2 is automatically obtained.

The selection of the transmissibilities of the branches will now be examined with reference to Fig.20. We begin with the symbols containing indices which do not belong to any neighboring joining line. This is the case with the transmissibility $|\overline{ae}| = |16|$ of the branch MN, the transmissibility $|ae| = |17|$ of the branch MP, the transmissibilities $|c| = |4\ 5|$, $|ad| = |9|$ of the branch MQ, and the transmissibility $|\overline{acde}| = |1\ 3|$ of the branch MR.

Then we apply rule 1 of Chapter 4.5.

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We enumerate the penetrations of the numerical symbols in the various closed circuits. We are interested in the penetrations of the circuits

$$MNPM = 2\ 8 \quad MPQM = 2 \quad MQRM = 0$$
$$MNQM = 2\ 4 \quad MPRM = 0$$
$$MNRM = 1$$

In the circuit MNRM we have already selected $|MR| = |a\bar{c}\bar{d}\bar{e}| = |13|$; it suffices to select further $|MR| = |ab| = |1\ 5\ 9\ 17|$ for satisfying $a\overline{bcde} = 1$ between the nodes M, N.

Similarly we select in the circuit MNQM the transmissibilities $|NQ| = |b| = |2\ 3|$, $|MN| = |\bar{a}b| = |2|$. With this we have satisfied the components of the transmissibility $\bar{a}b = 2$ between the nodes MQ (at this the selection is no longer unambiguous).

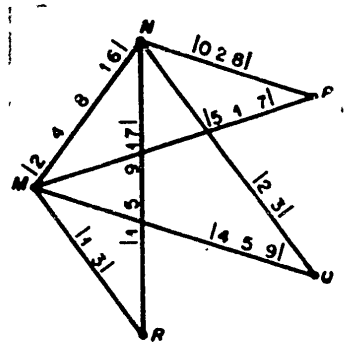

Fig.21 - Diagram of Transmissibilities of Networks

In the circuit MNPM we select $|\bar{a}d| = |8|$ as a further component of the transmissibility of the branch MN. If a relay with switching of contacts had not been contemplated, there would have been further selected the transmissibilities $|b|$, $|d|$ in the branch NP. For a relay with disconnection of the contacts, however, it is better to select $|NP| = |\overline{ace}| = |0\ 2\ 8|$, because the disconnection of the contacts $\bar{a}$, $\bar{c}$ has the supplements a, c, in the neighboring branch. Therefore, only one special contact $\bar{e}$ need be selected. This selection satisfies our components $\bar{a}b = 2$, $\bar{a}d = 8$ between the nodes M, P.

In the circuit MNQM we select the component $|MN| = |\bar{a}c|$.

Immediately after finishing the selection of the transmissibilities of the branches, we carry out the verification according to Chapter 3.1. The corresponding diagram of the transmissibilities of the branches is represented in Fig.21

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reader can easily form for himself the symbols of the transmissibilities of a network and compare it with this one.

For the verification it is ascertained whether the transmissibilities of the branches have the transmissibilities of the network given by the correct symbols wherever transmissibility is prescribed. The transmissibilities of the network between the other nodes are, however, distinguished from the transmissibilities which we have permitted. This, of course, is not according to rule.

5. Synthesis of Branches

The synthesis of the network is a working procedure which is regarded as the final selection of the transmissibilities of the branches. The transmissibilities which we get are not usually elementary; in the branches are connected not simple switch elements but more or less complicated relay switches.

The synthesis of such relay switches (synthesis of the branches) does not exactly fall in the framework of the present work. The remarks presented in this Chapter are limited to those necessary for completing the survey of the synthesis of the network. Without synthesis of the branches it is possible to proceed to the final phase of the synthesis of the network.

5.1 Statement of Problem of Synthesis of Branches. The diagram of the transmissibilities of the branches prescribes for each of the branches transmissibilities which are not usually elementary (I, $\emptyset$, a, $\bar{a}$, b, $\bar{b}$, ...). These are expressed by more or less complicated eqs.(3.3;1). If the relay switches whose transmissibilities were known are given by these expressions, they could be connected with the corresponding branches of the network, and the given problem would be solved. The connection and disconnection of the contacts of the relays, however, occurs only with the elementary transmissibility. Each of the branches must therefore be formulated like a network composed of branches of the elementary transmissibility.

The working procedure, which we call the synthesis of the branches, for the solution of the problem relating to the pair of nodes R, S of the given network is

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as follows.

The following are given:

1) The number n of components of the governed signals a, b, c, ...;

2) The transmissibility RS of the network between only one pair of nodes.

Add further the nodes T, U, V ... in such a way as to obtain a network whose transmissibilities of the branches are exclusively elementary.

This problem can be solved by methods known from several works. We may assume that the formation of relay switches from serioparallel branches on the basis of the structure of the algebraic expressions of the transmissibilities is known. We wish, however, to stress that the method of synthesis of the network outlined in the preceding chapter utilized expedients for simplifying the scheme obtained in the usual way. At the same time it is integrated with the picture of the whole problem of the synthesis.

For the discussion of the method for the synthesis of the branches, the concept of the maximal bridge was already mentioned.

5.2 Maximal Bridge. The synthesis of the branch RS is carried out at the synthesis of the network with the nodes R, S, T, U, V ... . Contrary to the problem which we have solved in Section 4, only one transmissibility of the network RS is prescribed here. At the application of this method to a network formulated in the usual way from the algebraic expressions of the transmissibilities, our first problem is to determine the permissible transmissibilities of the network. Although it would be the best procedure theoretically, we shall not construct here the usual developed diagram of the prescribed transmissibilities of the network, in which the maximal permissible transmissibilities for all of the pairs of nodes would be determined. Instead, we shall usually select only one pair of nodes T, U and select for it the transmissibility of the network expressed by the greatest possible number of values of the state index. This prescribed transmissibility of the network we shall call the maximal bridge TU_{max}.

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The maximal bridge is formulated by solution of the following problem:

In the network with the nodes R, S, T, U, V ... we have prescribed:

1) the transmissibility of the network RS;

2) the transmissibilities of the branches |RT|, |RU|, |UV|, etc.

Formulate the highest permissibility of the network TU_{max} between any selected nodes T, U in such a way that it consists of the greatest possible number of indices of transmissibility but without changing the transmissibility of the network RS.

Solution of problem: By shortcircuiting the nodes T, U (we assume |TU|)=I) the transmissibility of the network between the nodes R, S is increased from the original value RS to the value RS', which is usually by several numerical elements richer than RS. It is easy to see that this is just the index which we dare not permit in the transmissibility of the bridge. The prohibited index is therefore obtained as the penetration of the symbol RS' with the supplement $\overline{RS}$ of the original transmissibility RS:

$$\overline{RS} \,.\, RS' \qquad (5.2;1)$$

Finally, the highest transmissibility which we may permit in the bridge is the supplement of this expression, so that

$$TU_{max} = RS + \overline{RS'} \qquad (5.2;2)$$

The bridge is therefore composed of the transmissibility RS prescribed between R, S, to which we assign the index for which the network is transmissive between the nodes R, S shortcircuited with TU.

5.3 Example of Synthesis of Branch. In the diagram of the transmissibilities of the branches obtained by the synthesis of a given network let the transmissibility be prescribed for the branch RS:

$$|RS| = ae + abd\bar{e} + ade + bce + cd\bar{e} \qquad (5.3;1)$$

0 2 4 6 11 12 13 14 15 17 19 21 22 23 25 27 29 30 31

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We seek the network with the nodes R, S, T, U ... , with only the prescribed transmissibility of the network RS. First let us try to arrange the algebraic

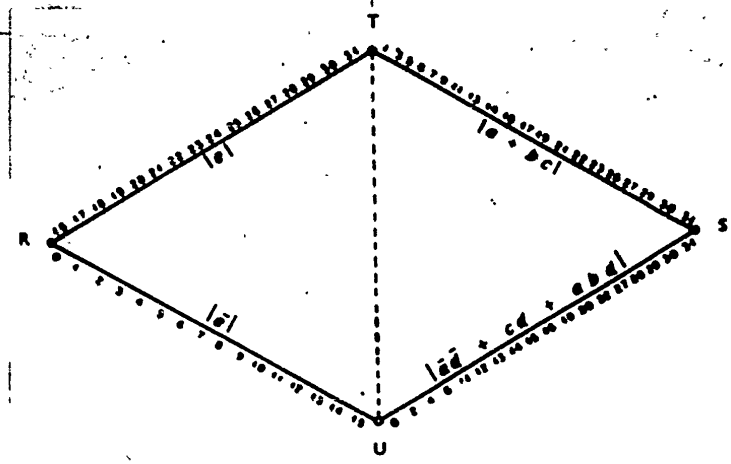

Fig.22

expression. It is sufficient to be familiar with only the general form of the arrangement:

$$\begin{array}{c} a(.+.)+c(.+.)+\ldots \quad b(.+.)+e(.+.)+\cdot \\ c(.+.)+e(.+.)+\ldots \quad d(.+.)+e(.+.)+\cdot \\ e(.+.)+\bar{e}(.+\cdot+.) \end{array} \qquad (5.3;2)$$

The last arrangement gives only two parallel branches. Therefore we denote it by the expression

$$RS = e(a + bc) + \bar{e}(abd + ad + cd). \qquad (5.3;3)$$

Figure 22 represents according to this expression the diagram of the transmissibilities of the branches with the network R, S, T, U, which has prescribed the transmissibility of the network RS. For this, two nodes T, U remain between which the branch is nontransmissive. We are interested in the maximal transmis[illegible]y which

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we may permit in this branch. The maximal bridge between the nodes T, U determined according to the preceding Chapter is

$$TU_{max} = RS + (8\ 10\ 24\ 26)$$
$$= 0\ 2\ 4\ 6\ 8\ 10\ 11\ 12\ 13\ 14\ 15\ 17\ 19\ 21\ 22\ 23\ 24\ 25\ 26\ 27\ 29\ 30 \qquad (5.3;4)$$
$$= \overline{ac} + ac + (11\ 13\ 15\ 22\ 24\ 26\ 30)$$

According to this expression we may permit a transmissibility of the network $TU = ae + \overline{ae}$. The selected transmissibility in the branch TU may contain either of these components or both. The transmissibility of the found bridge is noted on the diagram at the corresponding joining line. Because this is a permissible transmissibility of the network, we do not put it in parentheses. It is easy to see that we dare not use the whole maximal bridge. We usually use only the part thereof expressed by the simplest possible Boolian symbol.

For the practical execution of the synthesis we construct Fig.22. It is much more convenient and efficient to compose the diagram of the numerical bones as represented in Fig.23. In this way we gain two great advantages. First, we need not write out the numerical symbols, and second, the bones can easily be moved around for quickly re-arranging the diagram.

At this the transmissibilities of the network can easily be investigated, and we investigate the maximal bridges between many pairs of points and at the most diverse variants of the diagram. The found bridge represents only a permissible transmissibility of the network, which we may use but need not adopt; therefore, the bridge is at first noted only tentatively on the simple draft of the network; therefore, the bridge between the nodes T, U which we have found is noted only tentatively. Whether the selection of the transmissibilities $|ae|$, $|\overline{ae}|$ in the branch TU would not enable simplification of the transmissibility in some other branch has also been investigated.

Another maximal bridge is sought between the nodes U, V of the network, which

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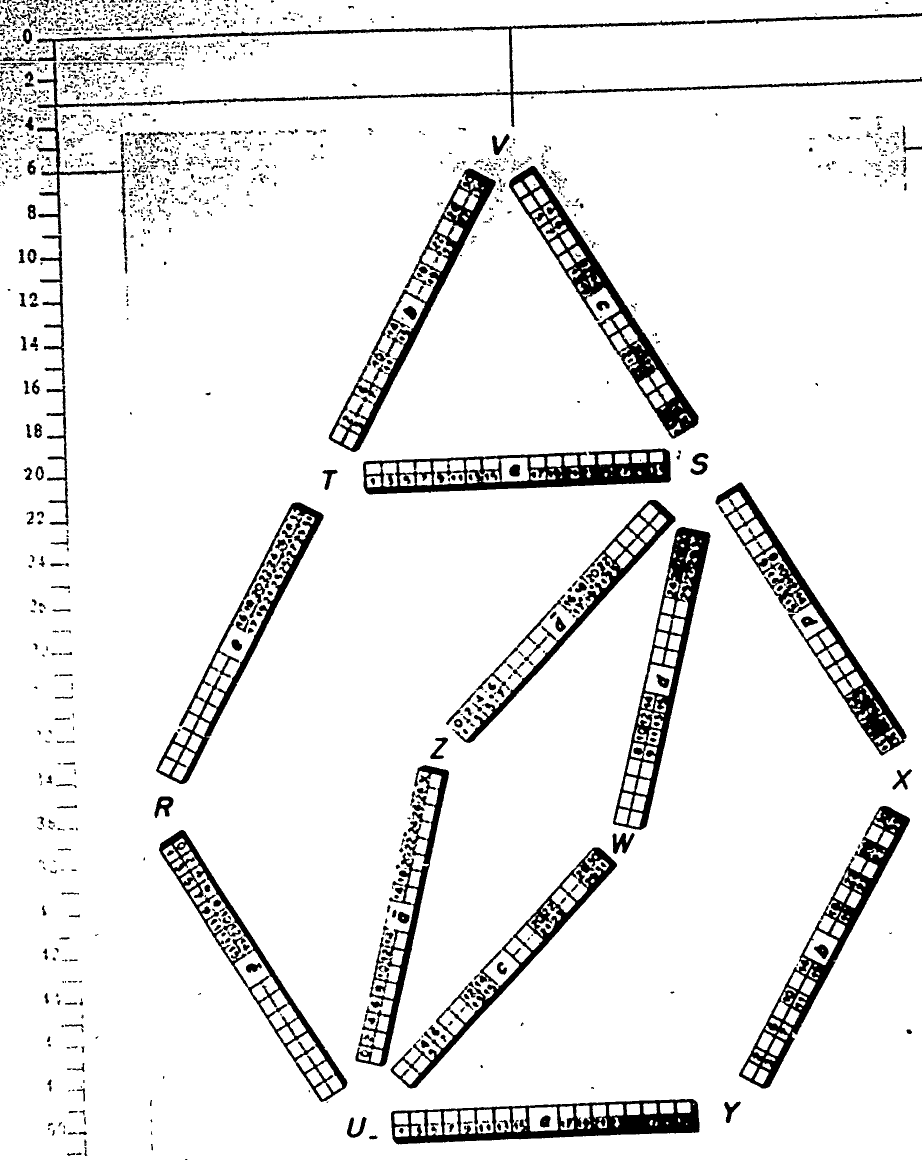

Fig.23 - Model of Network Composed of Numerical Bones

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is represented in Fig.23. The bones are re-arranged in such a way that the points U, V coincide. Then we ascertain for which index the network is nontransmissive between the nodes R, S. We find the index

1 8 9 10 16 20 24 26 28

and therewith the bridge.

$$UV_{max} = 0\ 1\ 2\ 4\ 6\ 8\ 9\ 10\ 11\ 12\ 13\ 14\ 15\ 16\ 17\ 19\ 20\ 21\ 22\ 23\ 24\ 25\ 26\ 27\ 28\ 29\ 30\ 31 + d + \text{(remainder)}$$

When we try to select the transmissibility of the branch $|UV| = |d|$ we see according to Fig.24 that for de = 1 the nodes S, U are already joined by the path SVU, so that the path SWU is superfluous*. Similarly, we see that if abd = 1 the nodes S, U are joined by the path STVU, so that the path SXYU is superfluous.

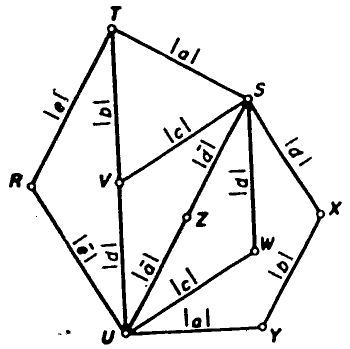

Fig.24 - Connection of Maximal Bridge

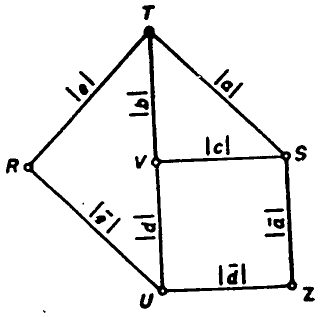

Fig.25 - Definitive Scheme of Branch RS

Already the second bridge which we found led to a favorable simplification of the circuit (Fig.25). Of course, this does not mean that we have found the only

* We can also apply rule 1, Chapter 4.5.

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possible solution. However, this solution is satisfactory for our practical purposes, and also enables elimination of some switching contacts (which are assumed for the relays here).

6. Definitive Synthesis of Network

A detailed description of this working procedure will be published in a separate work. This chapter is to be regarded only as a preliminary report. We present it only for supplementing the information on the method of synthesis discussed in this work.

We repeat some of the main points of the whole method of synthesis:

The main nodes M, N, P ... of the network are given and between them the transmissibilities in dependence on the state index are prescribed.

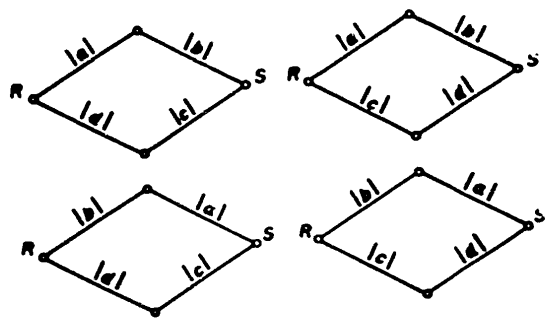

Fig.26 - Equivalent Variants

With the help of the developed diagram of the prescribed transmissibilities, we determine the permissible transmissibilities of the network and construct the corresponding maximal diagram of the transmissibilities of the network.

The maximal diagram of the transmissibilities of the network is algebraized.

With the transmissibilities of the branches we construct (according to certain rules) the diagram of the transmissibilities of the branches.

If all of these transmissibilities are elementary, we construct the network

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by synthesis. If this is not the case, we carry out the synthesis of all of the branches. By joining the formed branches between the main nodes of the network we begin the definitive synthesis of the network, as briefly described in the next paragraph.

Already, before interposing the formed branches between the corresponding main nodes of the network, we usually ascertain whether we cannot obtain several equivalent variants by regrouping of the branches. In Fig.26 we see an example of equivalent schemes of the branch RS. At the definitive synthesis each of the possible variants must be considered, because usually each of them leads to a different resultant network.

If the variants of the individual branches of the network are denoted by the numbers v_1, v_2 ... the total number of network diagrams which can be constructed from them will be given by the product $v_1 \cdot v_2$ ... of these numbers.

The number of these diagrams is so great that it is advisable to seek some rule for the selection of the variant of the branches. Here we only have space to say that this rule consists in concentrating on which nodes of the elementary transmissibilities are either concordant or supplementary.

After finishing the selection of the variants of the branches we proceed with the network, which will contain besides the main nodes M, N, P ... also the subsidiary nodes T, U, V ..., and with which all of the branches will have the elementary transmissibility.

However, this diagram does not usually represent a solution with an economical small number of contacts. Theoretically, the network should also contain the nodes T, U, V ... on the basis of the detailed methodical synthesis of the network. There would have had to be determined the developed diagrams of the transmissibilities of the branches, constructed therefrom the maximal diagram of the transmissibilities of the network, carried out a new selection of the transmissibilities of the branches, particularly of the branches which were previously nontransmissive.

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These new selected transmissibilities would then be as much as possible elementary or at least very simple (algebraically).

Instead of this method, which is theoretically the most correct but rather time-consuming, we are satisfied with a method which is less correct but very often satisfactory; we calculate the maximal bridges between the pairs of nodes of the network, particularly between the pairs of subsidiary nodes. As soon as we connect, with a maximal bridge, the elementary transmissibility we include it in the diagram as a new transmissibility of the corresponding branch, and then seek the next bridge on the assumption that a new branch is practicable. In this way we try to form a network with the largest possible number of bridges with the elementary transmissibility.

The definitive arrangement of the diagram of the transmissibilities of the branches is carried out by its development. For each i we determine which branches form the prescribed transmissibilities of the network, and we ascertain separately the double and multiple paths. The fact that one path is sufficient for the formation of the prescribed transmissibilities of the network follows from the conditions for the definitive selection of the transmissibilities of the branches, which are often expressed in the form of simultaneous equations of Boolian algebra. If the problem is too complicated, it can be solved by machine.

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SUMMARY

A method is described for the synthesis of relay contact networks whose transmissibilities are prescribed tabularly. The contact network formed may have any number of terminals and prescribed transmissibilities for any number of pairs of said terminals.

In the introduction, the concept of numerical symbol (a, b,...$\bar{a}$, $\bar{b}$,...) is presented. These are explicitly written sets of integers. It is then proved that operations with these sets are isomorphous with operations on variables of Boolean algebra.

In Chap.2 it is shown how to describe the transmissibility of the network between two terminals P, Q as a function of the index of state i. All possible states of the network are suitably numbered. Those states in which the network is transmitting between the terminals P, Q are then expressed by a numerical symbol composed of the indexes of state used to denote these states. The elementary numerical symbols corresponding to the variables a, b, ..., $\bar{a}$, $\bar{b}$, ..., used in Boolean algebra, are defined and given once and for all.

In Chap.3 it is shown how the numerical symbols are used in the analysis of a given relay contact network. Numerical strips (bones) are described for use as graphico-mechanical aids in analysis and synthesis. The use of tables for transforming the numerical symbols into algebraic form is also described in this place.

In Chap.4, finally, the new method of relay network synthesis is described. An

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important step here is the completion of the network transmissibility matrix. The transmissibility of network branches is then chosen according to two basic theorems. In this way algebraic expressions are obtained according to which individual branches of the network are designed as series-parallel contact circuits.

In the remaining chapters the method of branch synthesis on the basis of the concept of maximum bridge between two arbitrary nodes is described. The complete synthesis of the relay contact network is briefly outlined.

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TABLES OF NUMERICAL SYMBOLS

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32	a	1		3		5		7		9		11		13		15		17		19		21		23		25		27		29		31	a
33	a ē	1		3		5		7		9		11		13		15																	a ē
34	a d̄	1		3		5		7										17		19		21		23									a d̄
35	a d̄ ē	1		3		5		7																									a d̄ ē
36	a c̄	1		3						9		11						17		19						25		27					a c̄
37	a c̄ ē	1		3						9		11																					a c̄ ē
38	a c̄ d̄	1		3														17		19													a c̄ d̄
39	a c̄ d̄ ē	1		3																													a c̄ d̄ ē
40	a b̄	1				5				9				13				17				21				25				29			a b̄
41	a b̄ ē	1				5				9				13																			a b̄ ē
42	a b̄ d̄	1				5												17				21											a b̄ d̄
43	a b̄ d̄ ē	1				5																											a b̄ d̄ ē
44	a b̄ c̄	1								9								17								25							a b̄ c̄
45	a b̄ c̄ ē	1								9																							a b̄ c̄ ē
46	a b̄ c̄ d̄	1																17															a b̄ c̄ d̄
47	a b̄ c̄ d̄ ē	1																															a b̄ c̄ d̄ ē
48	b			2	3			6	7			10	11			14	15			18	19			22	23			26	27			30	31	b
49	b ē			2	3			6	7			10	11			14	15																b ē
50	b d̄			2	3			6	7											18	19			22	23								b d̄
51	b d̄ ē			2	3			6	7																								b d̄ ē
52	b c̄			2	3							10	11							18	19							26	27				b c̄
53	b c̄ ē			2	3							10	11																				b c̄ ē
54	b c̄ d̄			2	3															18	19												b c̄ d̄
55	b c̄ d̄ ē			2	3																												b c̄ d̄ ē
56	ā b			2				6				10				14				18				22				26				30	ā b
57	ā b ē			2				6				10				14																	ā b ē
58	ā b d̄			2				6												18				22									ā b d̄
59	ā b d̄ ē			2				6																									ā b d̄ ē
60	ā b c̄			2								10								18								26					ā b c̄
61	ā b c̄ ē			2								10																					ā b c̄ ē
62	ā b c̄ d̄			2																18													ā b c̄ d̄
63	ā b c̄ d̄ ē			2																													ā b c̄ d̄ ē

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64	ab	3 7	11 15	19 23 27 31	ab
65	$ab\bar{e}$	3 7	11 15		$ab\bar{e}$
66	$ab\bar{d}$	3 7		19 23	$ab\bar{d}$
67	$ab\bar{d}\bar{e}$	3 7			$ab\bar{d}\bar{e}$
68	$ab\bar{c}$	3	11	19 27	$ab\bar{c}$
69	$ab\bar{c}\bar{e}$	3	11		$ab\bar{c}\bar{e}$
70	$ab\bar{c}\bar{d}$	3		19	$ab\bar{c}\bar{d}$
71	$ab\bar{c}\bar{d}\bar{e}$	3			$ab\bar{c}\bar{d}\bar{e}$
72	c	4 5 6 7	12 13 14 15	20 21 22 23 28 29 30 31	c
73	$c\bar{e}$	4 5 6 7	12 13 14 15		$c\bar{e}$
74	$c\bar{d}$	4 5 6 7		20 21 22 23	$c\bar{d}$
75	$c\bar{d}\bar{e}$	4 5 6 7			$c\bar{d}\bar{e}$
76	$\bar{b}c$	4 5	12 13	20 21 28 29	$\bar{b}c$
77	$\bar{b}c\bar{e}$	4 5	12 13		$\bar{b}c\bar{e}$
78	$\bar{b}c\bar{d}$	4 5		20 21	$\bar{b}c\bar{d}$
79	$\bar{b}c\bar{d}\bar{e}$	4 5			$\bar{b}c\bar{d}\bar{e}$
80	$\bar{a}c$	4 6	12 14	20 22 28 30	$\bar{a}c$
81	$\bar{a}c\bar{e}$	4 6	12 14		$\bar{a}c\bar{e}$
82	$\bar{a}c\bar{d}$	4 6		20 22	$\bar{a}c\bar{d}$
83	$\bar{a}c\bar{d}\bar{e}$	4 6			$\bar{a}c\bar{d}\bar{e}$
84	$\bar{a}\bar{b}c$	4	12	20 28	$\bar{a}\bar{b}c$
85	$\bar{a}\bar{b}c\bar{e}$	4	12		$\bar{a}\bar{b}c\bar{e}$
86	$\bar{a}\bar{b}c\bar{d}$	4		20	$\bar{a}\bar{b}c\bar{d}$
87	$\bar{a}\bar{b}c\bar{d}\bar{e}$	4			$\bar{a}\bar{b}c\bar{d}\bar{e}$

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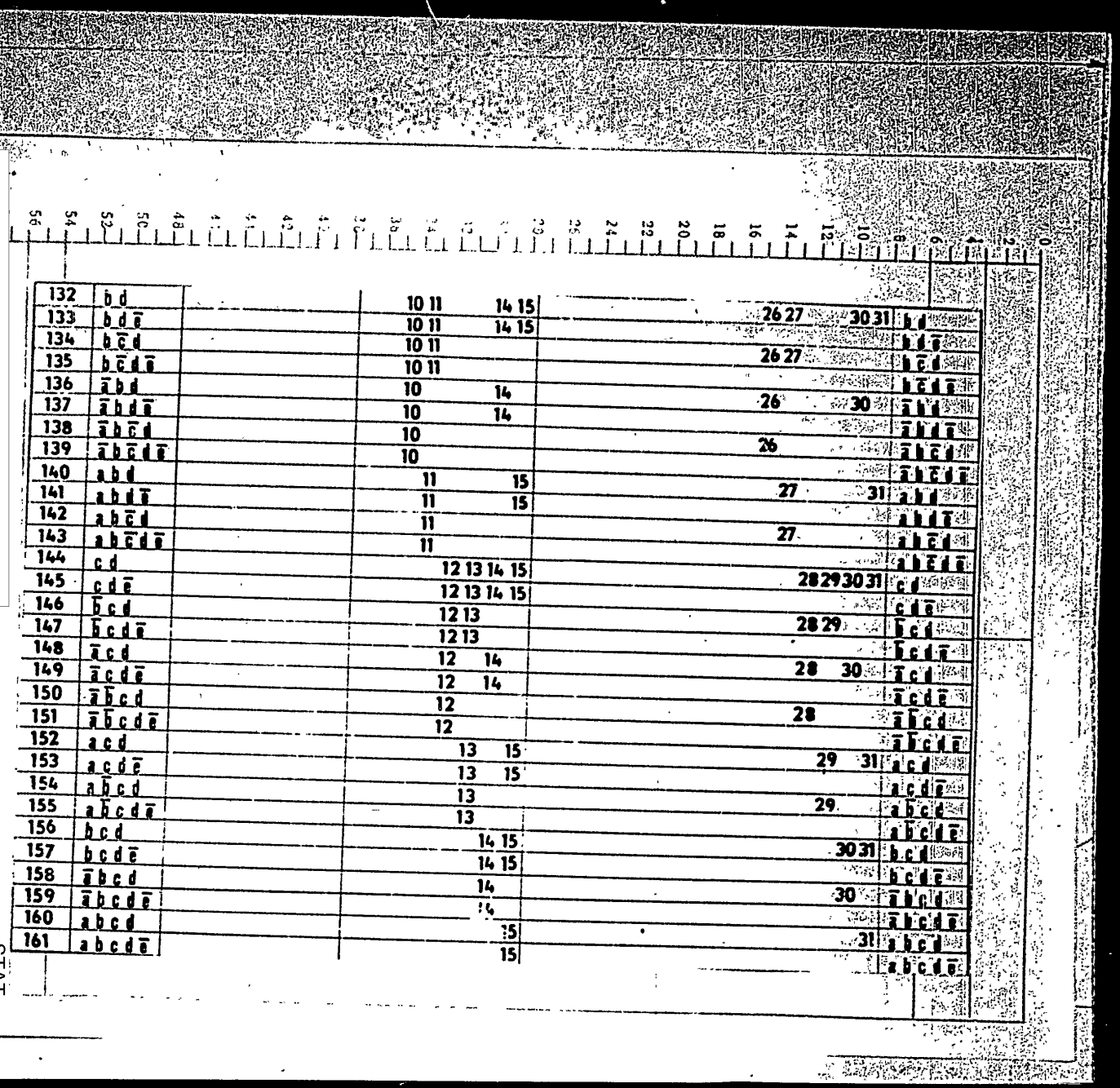

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162	e	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
163	d̄e	16 17 18 19 20 21 22 23
164	c̄e	16 17 18 19 24 25 26 27
165	c̄d̄e	16 17 18 19
166	b̄e	16 17 20 21 24 25 28 29
167	b̄d̄e	16 17 20 21
168	b̄c̄e	16 17 24 25
169	b̄c̄d̄e	16 17
170	āe	16 18 20 22 24 26 28 30
171	ād̄e	16 18 20 22
172	āc̄e	16 18 24 26
173	āc̄d̄e	16 18
174	āb̄e	16 20 24 28
175	āb̄d̄e	16 20
176	āb̄c̄e	16 24
177	āb̄c̄d̄e	16
178	ae	17 19 21 23 25 27 29 31
179	ad̄e	17 19 21 23
180	ac̄e	17 19 25 27
181	ac̄d̄e	17 19
182	ab̄e	17 21 25 29
183	ab̄d̄e	17 21
184	ab̄c̄e	17 25
185	ab̄c̄d̄e	17
186	be	18 19 22 23 26 27 30 31
187	bd̄e	18 19 22 23
188	bc̄e	18 19 26 27
189	bc̄d̄e	18 19
180	āb̄e	18 22 26 30
181	āb̄d̄e	18 22
192	āb̄c̄e	18 26
193	āb̄c̄d̄e	18

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194	a b e	19 23 27 31	a b e
195	a b $\bar{d}$ e	19 23	a b $\bar{d}$ e
196	a b $\bar{c}$ e	19 27	a b $\bar{c}$ e
197	a b $\bar{c}$ $\bar{d}$ e	19	a b $\bar{c}$ $\bar{d}$ e
198	c e	20 21 22 23 28 29 30 31	c e
199	c $\bar{d}$ e	20 21 22 23	c $\bar{d}$ e
200	$\bar{b}$ c e	20 21 28 29	$\bar{b}$ c e
201	$\bar{b}$ c $\bar{d}$ e	20 21	$\bar{b}$ c $\bar{d}$ e
202	$\bar{a}$ c e	20 22 28 30	$\bar{a}$ c e
203	$\bar{a}$ c $\bar{d}$ e	20 22	$\bar{a}$ c $\bar{d}$ e
204	$\bar{a}$ $\bar{b}$ c e	20 28	$\bar{a}$ $\bar{b}$ c e
205	$\bar{a}$ $\bar{b}$ c $\bar{d}$ e	20	$\bar{a}$ $\bar{b}$ c $\bar{d}$ e
206	a c e	21 23 29 31	a c e
207	a c $\bar{d}$ e	21 23	a c $\bar{d}$ e
208	a $\bar{b}$ c e	21 29	a $\bar{b}$ c e
209	a $\bar{b}$ c $\bar{d}$ e	21	a $\bar{b}$ c $\bar{d}$ e
210	b c e	22 23 30 31	b c e
211	b c $\bar{d}$ e	22 23	b c $\bar{d}$ e
212	$\bar{a}$ b c e	22 30	$\bar{a}$ b c e
213	$\bar{a}$ b c $\bar{d}$ e	22	$\bar{a}$ b c $\bar{d}$ e
214	a b c e	23 31	a b c e
215	a b c $\bar{d}$ e	23	a b c $\bar{d}$ e
216	d e	24 25 26 27 28 29 30 31	d e
217	$\bar{c}$ d e	24 25 26 27	$\bar{c}$ d e
218	$\bar{b}$ d e	24 25 28 29	$\bar{b}$ d e
219	$\bar{b}$ $\bar{c}$ d e	24 25	$\bar{b}$ $\bar{c}$ d e
220	$\bar{a}$ d e	24 26 28 30	$\bar{a}$ d e
221	$\bar{a}$ $\bar{c}$ d e	24 26	$\bar{a}$ $\bar{c}$ d e
222	$\bar{a}$ $\bar{b}$ d e	24 28	$\bar{a}$ $\bar{b}$ d e
223	$\bar{a}$ $\bar{b}$ $\bar{c}$ d e	24	$\bar{a}$ $\bar{b}$ $\bar{c}$ d e

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EMPLOYMENT OF INDETERMINATE TWO-VALUE BOOLIAN FUNCTIONS FOR SYNTHESIS OF ONE-BEAT SWITCHING CIRCUITS*

by

Frantisek Svoboda

Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences

Received: November 14, 1953

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* Presented to Second Regular Whole-State Conference of Laboratory of Mathematical Machines in December 1953

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In the present article an inductive combinatory method is described for the synthesis of one-beat switch circuits with one input and m output poles, which, in contrast to the previous methods, does not utilize the theory of Boolian algebra. The method uses a simple symbolism. While it is described as a method for human manipulation it is also valid for machines, i.e., the method can by supplementary processes be adapted for solution of the problem by machine. It can be shown that according to the method it is possible to get to every possible structure of the solution of the problem. This method is the first which proceeds to the solution from the given functions in the output pole to the input pole. In this it differs from most of the previous methods, which start with some starting solution for proceeding deductively to the definitive solution by the simple process of successive improvement.

The method described is general to such an extent that it is applicable to any phase of the considered problem, and is characterized in that the same working process is continuous during the development of the solution. This fact, together with the expression of the indeterminate functions in tabular form enables the construction of a machine for automatic synthesis.

1. Introduction

1.1 Previous Methods. Let us discuss the previous method for the synthesis of multipoles with one input and m output poles. Shannon (Bibl.2) has published a method for the synthesis of 2-polar ($m = 1$) schemes, which he could not further increase to $m > 1$. In this method Shannon assumes that a part of the scheme forms a pyramid (disjunctive tree), and that this prevents in advance the construction of higher types of schemes which might be more advantageous under certain conditions. More recently Gavrilov (Bibl.3) has described a method for the synthesis of so-called arranged schemes. These schemes constitute a relatively small class of all schemes. On nonarranged schemes, of course, a number of experiments have been published. [illegible] has also described a fairly general method for the transformation of multi-

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poles. Recently, A.G.Lunc (Bibl.4) has described an algebraic method for the transformation of contact multipoles. The scheme with one input and m output poles is a special multipole. In this method Lunc follows Gavrilov's direction in the sense that he carries out the synthesis of a contact multipole by successive transformations of indeterminate starting multipoles. For this operation he uses the so-called characteristic functions of the matrices of the scheme. This method is noteworthy for the fact that it is probably the first fully-developed algebraic method which enables the construction of higher types of schemes. This method consists essentially in the transformation of the n-star to the n-triangle [(3), pp.214-217] and the opposite transformation, which are formulated algebraically. The first transformation corresponds exclusively to one variable of the characteristic function, while the second transformation adds a further variable to the characteristic function. In this method, however, Lunc does not discuss at all the question of the economy of the solution.

In conclusion it can be said that in the present state of the development of the methods, an extensive employment of the theory of Boolian algebra is characteristic. A number of modern works in this field exist whose authors are inaccessible; therefore the enumeration of the previous methods is incomplete.

1.2 Essence of Problem. We shall now examine the important question which represents the essence of the problem in this field. We shall also examine the known methods for the synthesis of one-beat circuits with one input and m output poles.

The main problems are essentially two; i.e., the question of the economy of the solution and the question of finding a general method for the solution of the problem which is applicable to the whole class of problems. Let us now examine these two problems in detail.

With regard to the economy of the solution, what is concerned here is that the number of structural elements is a certain minimum. For example, at the designing of a relay circuit there may have to be, for example, five switching contacts for

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each of the employed relays.

With the question of the economy in the considered sense, the question of the method of assembling the structural elements for the proposed scheme and that of the best utilization of these elements is closely connected.

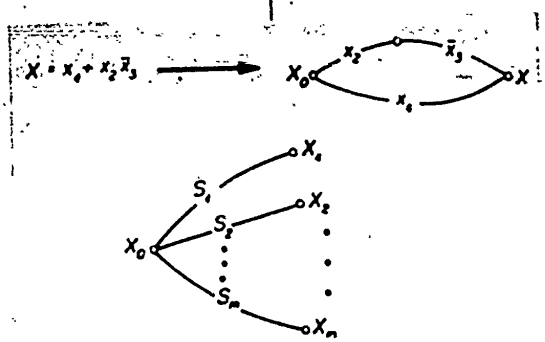

Fig.1.1 – Example of Serioparallel Scheme and Representation of Scheme with One Input and m Output Poles

Assume that we have to formulate a scheme of a multipole to whose m output poles are assigned the binary switch function $X_k = X_k(x_1, x_2, \ldots, x_i, \ldots, x_n)$ where x_i, $i = 1, 2, \ldots, n$ are binary variables. The function X_k, $k = 1, 2, \ldots, m$ is not a prescribed value.

The problem must be solved, for example, in such a way that for each of the functions we have some algebraic form thereof, and then depict all of them in the form of a serioparallel scheme (Fig.1.1).. Even if we simplify this form as much as possible in such a way that it contains the shortest possible notation "x_i", $x_i = x_i$ or x_i or $\bar{x}_i$, we again get only the algebraic form which represents the serioparallel scheme. The function X_k corresponds in Fig.1.1 to scheme S_k; X_0, the function assigned

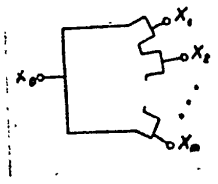

Fig.1.2

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to the input pole, as I.

It is found that this is not a very suitable method of synthesis. It is unsuitable because it does not utilize the immense combinatory possibilities of any arrangement of the structural elements. With the problems occurring in practice, we usually get a more advantageous solution of nonserioparallel schemes. From Bibl.5, for example, it follows that in the practical case where the main concern is p = = 30 - 40 - 50 elements, the share of the serioparallel circuits is small in comparison with all of the possible circuits which can be constructed from these elements. At p = 4 all of the schemes are serioparallel, at p = 9 the serioparallel schemes are only 60%, but at increasing p the share of the nonserioparallel scheme increases much more rapidly because of the great combinatory possibilities.

Higher types of arrangements have been systematically investigated by Gavrilov (Bibl.3) and by Lunc (Bibl.4). He states with respect to the method for determining the functions from the algebraic forms the fact that these functions represent several bridge schemes. He also presents, in Chapter 10 of Bibl.3, a number of rules for arranging the schemes according to "various connecting methods". The improved method of Lunc develops constructions of schemes of very general structure.

We can also get more economical schemes by formulating the parts not as represented in Fig.1.1 but in such a way that some of the schemes are common to all or some of the schemes formed by the function X_k, k = 1, 2, ..., m.

From this it is directly clear that we eliminate some of the schemes which are common. Although the literature contains some references to the solution of this problem, the latter has not heretofore been systematically investigated.

On the other hand, the finding of a method leading to an economical solution which is applicable to the whole class of problems is also concerned. This problem is closely connected with the theory of algorithm and with mechanical solution of problems of synthesis.

An algorithm, i.e., a method of solving problems which assures a minimal number

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of structural elements, is not yet known. There seem to be many reasons why it has not so far been possible to formulate such a method. Such a procedure is not possible in the present stage of any of the methods.

Thus, for example, Shannon (Bibl.2), before the construction of the scheme, divides the variables of the switch function into two groups: the variables of the first group correspond in the scheme to pyramids, while the variables of the second group with some serioparallel schemes are connected with the individual outputs of the pyramids. At this, Shannon fails to state how to divide the variables into these two groups. There are many possibilities. Lunc's method operates with the characteristic functions of the matrices of the scheme. Here some of the variables are rejected and others accepted. However, as Lunc states, the introduction of the variables in the problem is ambiguous, and he fails to give the directions for their introduction in such a way as to obtain the solution in the required form.

Unsolved remains precisely the problem of a general method for an economical solution. A system of methods is usually employed for the solution of a particular class of problems or rules and recommended artifices, which are employed in this or that case, i.e., at particular parts of the problem, or in a particular form of the solution. For example, Gavrilov gives for the arrangement of the schemes with various methods of connecting about 20 rules, which we have managed to simplify. Lunc, on the other hand, gives a general method, but this method is wholly unrelated to the question of the economy.

This problem is closely connected with the mechanical concept of the problem. The method adopted for the machine must be sufficiently general and simple, because this particularity is inherent in the conception of the machine. Such a method is so far lacking.

1.3 Outline of Problem Solved in This Work. This work is devoted to the two preceding questions, i.e., to the question of the economy of the solution and to the problem of finding a general method to an economical solution. Unsolved, how-

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ever, is the problem of the algorithm of the method for the most advantageous solution. A considerable influence was exerted on the clarification of this problem, among other things, by the written algebraic form of the switch function with the intermediate nodes of scheme, as described in the unpublished method utilizing symmetrical differences of A.Svoboda in 1950. It will be seen presently that it is precisely the intermediate nodes and their function to which particular attention in devoted in the present work.

The main tool is not the theory of Boolian algebra because of its fundamental shortcomings, which manifest themselves particularly at the arrangement of the structural elements (Bibl.1). The method described below has a combinatory character. The binary functions used for the formulation are arranged in tabular form (Bibl.1)* (except in a few cases expressed by the function $\sum$ -branches). Because usually not all of the functional values are defined, we speak of indeterminate binary functions.

On the First Problem: With the described combinatory method the arrangement of the structural element is, as it were, arbitrary. The circumstance is limiting that sometimes a particular structure element is not present in the connected sense (connection does not change the state of the scheme), or sometimes connection would lead to an incorrect solution. The method of arrangement of the elements does not depend at all on the algebraic form of the given function but on the local characteristic of the scheme in which we want to include it. The possibilities are very many, but, due to the indeterminate function, they can be surveyed relatively easily. This gives us the assurance to a certain extent that we usually have the possibility

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*The employment of such a form for the synthesis of switch circuits was presented for the first time by the author of present articles to the discussion of the Laboratory of Mathematical Machines on 24 October, 1952 with reference to the combinatory method.

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of a suitable selection of the successive operations for finding a suitable solution.

Finally, a partial solution of question at the utilization of structural element is enabled, on the one hand, by the employment of the indeterminate functions, and, on the other hand, by working backward from what is given (see Fig.1.3). This is at first glance illogical, but has the advantage here that we have from the beginning something on which to go, i.e., the output function X_k. In the initial stage we know only the functions in the output pole and in the input pole. If we were to begin the construction of the scheme with the input pole we would have too much uncertainty in the selection of the structural elements.

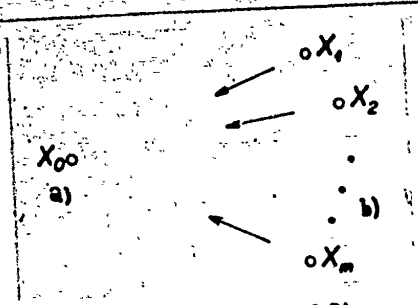

Fig.1.3 - Representation of Direction of Construction of Scheme
a) Input pole; b) Output poles

On the Second Problem: The method of solution indicated in the method is general to such an extent that it is applicable to any part of the problem of the synthesis of one-beat schemes and to every stage of the solution of the given problem.

The author indicates the general direction to be followed getting as close as possible to the required form of the solution. Although the method does not include a precise procedure - algorithm, we carried out in every stage of the solution a further operation, and approach the final solution by successive evaluations. For the solution, however, there are stages where the evaluating operation is difficult. The solution is carried out by a series of trials. At each trial we construct the complete solution. The greater the number of trials, the greater is the probability of getting a better result. The quality of the solution also depends to a considerable extent on the skill of the operator. From this viewpoint, therefore, the combinatory method is an experimental or inductive method.

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2. Fundamental Concepts and Definitions

The fundamental concepts and definitions are introduced for several reasons. On the one hand, they are used in the rest of this article, and on the other hand, there is no Czech terminology of the nomenclature, so that we are compelled to introduce some new concepts, as, for example, the mathematical definitions of supersonic and uniform subschemes.

At the introduction of the concepts we start with the world of physics, and, after abstraction, proceed to the mathematical concepts.

A terminal, or several terminals connected together by an electrical conductor, we call a node. A node is denoted schematically as a point.

A switch is a physical arrangement which dominates the electrical conductivity between two nodes U_1 and U_2. This is represented schematically in Fig.2.1.

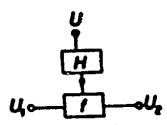

Fig.2.1

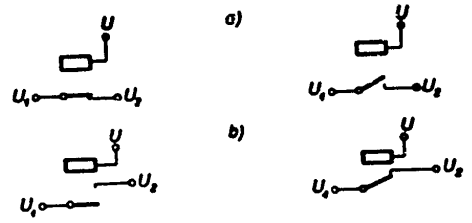

Fig.2.2

This conductivity has two states: either the two nodes U_1 and U_2 are electrically insulated from each other, so that the switch does not conduct, or the two nodes are electrically connected with each other in some way* so that the switch conducts.

As the example we take the relay with contact, and explain all of the concepts

* Switch is defined here not only as symmetrical physical arrangements, for example, relay with contact, by which the nodes U_1 and U_2 are switched, but also unidirectional electronic switches, etc.

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with reference thereto.

The switch may be present in two states: either in the resting state, in Fig.2.2a and b on the left, or in the working state, in Fig.2.2a and b on the right. The switch is brought from the resting state to the working state by means of the node U (due to the fact that the terminal U conducts electrical current to the relay).

In Fig.2.2a we represent the two states of a switch of the first type - relay with disconnector of contact. When this switch is in the resting state the two nodes U_1 and U_2 are connected with each other, and when it is in the working state, Fig.2.2a on the right, the two nodes are insulated from each other.

Figure 2.2b represents the two states of a switch of the second type - relay with connector of contact. When this switch is in the resting state, Fig.2.2b on the left, the two nodes U_1 and U_2 are insulated from each other, and when it is in the working state, Fig.2.2b on the right, the two nodes are connected with each other.

We see that the conductivity between the nodes U_1 and U_2 has two states, depending on the state in which the switch is present and on the type of switch. For the state of the switch we introduce the variable H and for the type of switch T. The conductivity f is therefore a function of the two arguments (T, H); all of the variables acquire the values (0, I).

$$f(T, H) = f. \tag{2.1}$$

The first type (relay with disconnector of contact T = 0) connects in the resting state (H = 0) the nodes U_1 and U_2:

$$f(0, 0) = I.$$

The second type (relay with connector of contact T = I) insulates from each other in the resting state (H = 0) the nodes U_1 and U_2:

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$$f(I, 0) = 0.$$

When the switches are in the working state (H = I) the first type insulates; the second type connects the nodes:

$$f(0, I) = 0$$
$$f(I, I) = I.$$

For survey the function f is presented in the form of the following Table, which also gives its algebraic forms:

T	H	f
0	0	1
1	0	0
0	1	0
1	1	1

$$TH + \overline{T}\,\overline{H} = f$$

Fig.2.3 - Table of Function f of Conductivity of Switch

The functional dependence (2.1) can be formed by a simpler method. This simplification is made because it is unnecessary to complicate the problem with the kind of switch and its state besides the conductivity. This is important when working with the physical arrangements in which the switch occurs but not at its formulation or construction with the help of the scheme. Between the state of the switch H and the conductivity f the following simple relation is also valid: with the switch of the second type, the values corresponding to the conductivity and the state of the switch follow from the formula, while with the switch of the first type these values are supplementary. Instead of the T and H the single variable x, ($\overline{x} = I - x$) can be introduced in such a way that we can express with it both the type and the state of the switch. If we introduce the binary variable x and assign it to the second type of switch and its supplemented variable $\overline{x} = I - x$ to the first type of switch,

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then we may write simply:

$$f(T, H) = f = \bar{x}, \text{ kde } \bar{x} = x \text{ nebo } \bar{x}.$$

Example: The switch of the first type has a conductivity of the given function $f_1 = \bar{x}$. We have at first the switch in the resting state (H = 0) according to eq.(2.1)', at which the switch of the second type disconnects the terminals $f_2 = 0 = x$, so that $\bar{x} = I - x = I = f_1$; the switch of the given type connects the terminals U_1 and U_2 and conversely when the switch is in in the working state (H = I).

x	f_1	f_2
0 I	I 0	0 I

Fig.2.4

The method described in this article is determined for the so-called symmetrical switch with the following characteristics:

If f = I is valid, then the statement is valid: "nodes U_1 and U_2 are connected by a conductive (in the physical sense nearly without resistance) connection", i.e., we get electrical voltage at both the node U_1 and node U_2, and conversely;

a)

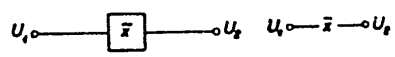

Fig.2.5 - Switch Elements

a) Abbreviation

The simplest type of symmetrical switch is the relay with contact.

The connection of the nodes U_1 and U_2 dominated by the switch is represented schematically in Fig.2.5.

The switch elements with the function f = x constitute the fundamental element of the switch scheme, which we call briefly the switch element x.

We proceed next with the definition of the switch scheme.

Consider now a wholly definite set $\mathcal{E}$ of switch elements x, i.e., a certain number of switch elements x and a certain number of switch elements $\bar{x}$. If H = 0 is valid, then all of the switch elements x are nonconductive and all of the switch

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elements x are conductive, and at H = I the converse. We have now a whole system of sets $\xi_1, \xi_2, \ldots, \xi_i, \ldots, \xi_n$, of which each set of switch elements ξ_i can always be independent of the remaining sets in one of the two possible states of conductivity. We have in all 2^n mutually different states of conductivity of the whole system.

The switch scheme is a definite set of points - nodes in space - connected with a definite system of sets of switch elements $\xi_1, \xi_2, \ldots, \xi_i, \ldots, \xi_n$ in such a way that at each of the nodes of the scheme at least one switch element starts. Every two nodes of the switch element coincide with some node of the definite set of nodes.

A subscheme of a switch scheme is a switch scheme each of whose nodes and each of whose switch elements belongs to the given switch scheme.

The branch of the given scheme between its nodes U_i and U_j is the maximal subscheme of the given scheme including the two nodes U_i and U_j.

With a continuous switch scheme or subscheme we can go from any of its nodes continuous with a switch element to any other node of the switch scheme or subscheme.

This brings us to the importance of the uniform subscheme (briefly: I-subscheme). The physical significance of the I-subscheme is as follows: Assume that we have a switch circuit in a particular state of conductivity: some of the switch elements are conductive, f = I, others are nonconductive, f = 0. As soon as electrical voltage at a particular node arrives, it also arrives at some other node. The whole part which is under voltage in this case is called the I-subscheme.

The I-subscheme is therefore the maximal subscheme at the particular state of the conductivity, at which it is possible to go from any of the nodes of any of the switch elements which are conductive, f = I, to any other node of the same subscheme.

Remarks: 1. When we speak of two I-subschemes of the same scheme we do so in the sense of two parts of the I-subscheme (it is impossible to go in the sense of the definition from one to the other).

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2. The I-subscheme is defined for a particular state of the conductivity of the scheme, i.e., for a particular state of the switch. The scheme can be divided for a particular state of the conductivity into several sets of I-subschemes, and for another state of the conductivity into another set of I-subschemes. In the following example the scheme has in the 1st state two I-subschemes and in the 2nd state three I-subschemes. Let us consider the I-subschemes for various states of the conductivity of the switch scheme. At n variables there are 2^n states.

$x_1 x_2 \ldots x_i \ldots x_n$		F
0 0 ... 0 ... 0	h_1	~
0 0 ... 0 ... I	h_2	~
. . ..	.	.
. . ..	h_j	.
. . ..	.	.
I I ... I ... I	h_{2^n}	~

Fig.2.7

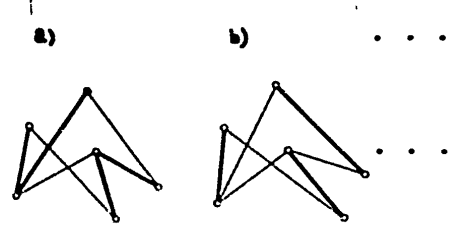

Fig.2.6 – Representation of I-Subscheme
a) 1st state; b) 2nd state

We introduce the following denotation for the combinations of the values of the argument: $h_j = (x_{j1}, x_{j2}, \ldots, x_{jn})$ (Fig.2.7), where $j = 1, 2, \ldots, 2^n$; then we put: $\{F(h_j)\}_{j=1}^{2n} = \{F\}$. When it is valid that the value of function F is for all of the combinations of the argument h_j equal to I or 0 (or I, see below) we shall denote this briefly in the form of $\{F\} = \{I\}$, or $= \{0\}$, or $= \{1\}$. Similarly, for the function f the symbol $\{f\}$. The symbol $\{F\}$ or $\{f\}$ then denotes the sequence of the functional values of the function $F(x_1, x_2, \ldots, x_i, \ldots, x_n)$ or $f(x_1, x_2, \ldots, x_i, \ldots, x_n)$ corresponding to the sequence of the combinations of the values of the argument compared according to magnitude (at which we regard this sequence of the values of the argument as binary expressions of numbers).

The switch function of the switch element will be called its functional conductivity $f = \tilde{x}$.

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Switch Function of Nodes in Scheme. To each of the switch elements in the scheme is assigned some switch function $f = \tilde{x}_i$, where $1 \leq i \leq n$. One of the nodes in the scheme is called input U_0. It is permanently under voltage, and its function is $\{X_0\} = \{I\}$. The switch function of the given node in the scheme is the function n of the binary argument $F = F(x_1, x_2, \ldots, x_i, \ldots, x_n)$, which has for each of the 2^n states of the conductivity of the scheme the values:

either I if the statement "given node is disconnected from input node" is valid;

or 0, if the statement "given node is connected to the input node" is valid.

The function F can be entered in Fig. 2.7. For the symbol heavy-wavy line, either 0 or I is obtained in the concrete case.

Remark: The function F depends mostly on the n of the argument.

The switch function of the branch $f = f(x_1, x_2, \ldots, x_i, \ldots, x_n)$ between the nodes U_1 and U_2 is equal to the switch function of one of its nodes when the other node is regarded as an input node. The function is therefore assigned to the pair of nodes which expresses the conductivity of the whole scheme between these two nodes.

The maximal continuity of the subscheme containing only the two given nodes U_1 and U_2, which is called its Σ-branch* is important. (For the exceptional case of $\{f\} = \{I\}$ these two nodes coincide according to definition. For $\{f\} = \{0\}$ the Σ-branch would be "empty".)

The branch thus defined is composed at the most of n parallel connections of switch elements with the function $f_i = \tilde{x}_i$, $1 \leq i \leq n$, $\tilde{x}_i = x_i$ or $\bar{x}_i$.

Example: We have $n = 5$, $f = x_2 + \bar{x}_3 + x_5$.

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* We call this the Σ-branch because its function f equals the sum of the conductivities of the switch elements contained in this branch.

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The construction of the function F with the help of the switch scheme in the particular node U will now be discussed with reference to the following problem: Construct for the given function F in the node U such a scheme that the switch function in the node U just equals the prescribed function F. In other words, at the place where the value I is prescribed for the function F, an I-subscheme must be formed which includes both the node U and the node U_0[which may also be regarded as the construction of the unit (I) of the function F, or briefly, as the construction of the unit I], and the place where the value 0 is prescribed must lie between the nodes U and U_0 in two I-subschemes.

We shall consider here in detail the I-subschemes with the node U. In the first case we shall speak of the I-subscheme with the value I, i.e., of the I-subscheme to all of whose nodes the value I is assigned, and in the second case of the I-subscheme with the value 0, i.e., to all of whose nodes the value 0 is assigned. For the sake of completeness we shall also wholly analogously speak of the I-subscheme with the indeterminate value ~ , or 1, or 1.

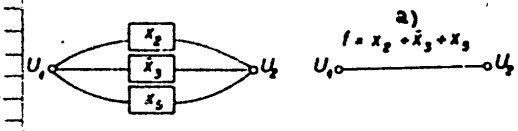

Fig.2.8 - Example of Σ-Branch

a) Abbreviation

The one-beat switch scheme* with one input U and m output nodes $U_1, \ldots, U_m$ is a continuous switch scheme, to whose one node (input pole) is conducted voltage and from whose m nodes (output poles) current is conducted. The remaining nodes in the scheme are called intermediate. The functions assigned to the output fields are denoted $x_1, x_2, \ldots, x_k, \ldots, x_m$; an operational table of the scheme is prepared.

* With the individual schemes the conductivity prevailing between the terminals is established by means of the state of the switch at one beat, and therewith the "work" of the end arrangement.

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For the proper procedure at the formulation of the scheme according to the method no errors are made. It should, however, be noted that for the definitive solution other functions than those originally intended* are assigned to the particular output poles. It should be noted that when the function X_k must be assigned to the kth output pole, the function $X'_k + X_k$ is assigned to it. We call the positive supersound or incremental function the function

$$+\Delta X_k = \overline{X}_k \cdot X'_k ,$$

and the negative supersound or decremental function the function

$$-\Delta X_k = \overline{X}'_k \cdot X_k .$$

3. Formulation of Problem

The binary functions X_k** are given where k = 1, 2, ..., m, in the form of the operational Table of the switch scheme represented in Fig.3.1.

$x_1 x_2 \dots x_i \dots x_n$	$X_1 X_2 \dots X_k \dots X_m$
0 0 ... 0 ... 0	? ? ... ? ... ?
0 0 ... 0 ... I	? ? ... ? ... ?
. . ..	. . ..
. . ..	. . ..
. . ..	. . ..
I I ... I ... I	? ? ... ? ... ?

Fig.3.1 – Operational Table

The content of the problem being given, we enter in the Table of Fig.3.1 for each symbol "?" one of the three symbols "~" or " I" or "0". If the value "~" is

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* The probability of errors is small because we always verify every operation. There are, however, methods at which errors can be made very easily, for example, the intuitive method.

** That is, some subsets of all 2^{2n} plural functions.

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prescribed, we do so regardless of the value of the function X_k, i.e., at the solution we can select between "0" and "1".

The Problem: Construct the one-beat switch scheme to whose m nodes the functions $X_1, X_2, \ldots, X_k, \ldots, X_m$ are assigned. The constructed scheme must have the smallest possible number of switch elements*.

For the structural elements we select the Σ-branches. The sum of the functions f of the Σ-branches is denoted Ω (of which there are $3^n - 1$). Form the important subsets of all of the possible functions Ω (of which there are 2^{2n}), Fig.3.2

Let us now consider one of the prescribed functions X_k, for example, X_{k_1}. If $X_{k_1} \varepsilon \omega$ is valid, then one Σ-branch with the function $f = X_{k_1}$ is sufficient for the formation X_{k_1}. If $X_{k_2} \varepsilon \Omega$ or $X_{k_2} \varepsilon \omega$ is valid, then, of course, there is insufficient for the formation of the function X_{k_2} any of the Σ-branches alone. It is usually necessary for the construction of the function X_{k_2} to take at least two Σ-branches, and hence to bring intermediate nodes into the scheme.

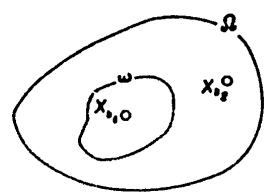

Fig.3.2

4. Ambiguities in Theory of Switch Circuits

We have several switch circuits in a definite state of conductivity. They correspond to the switch schemes represented in Fig.4.1, in which the I-subschemes are analyzed in a definite way. Let us consider any two nodes of these schemes U_i and U_j, to which are assigned certain values of the function $F_i(x_1, x_2, \ldots, x_n)$ and $F_j(x_1, x_2, \ldots, x_n)$ depending on whether for the given state of the conductivity

* This requirement is clearly weaker than the strict requirement "minimal number of switch elements of the scheme". The weaker requirement is made because what we are describing here is not the method of obtaining the best solution but only the best possible solution.

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the considered nodes are or are not under voltage. Consider further the function $f(x_1, x_2, \ldots, x_n)$ of the branch between the nodes U_i and U_j. To this function is likewise assigned a certain value depending on whether the branch conducts or whether the nodes U_i and U_j are disconnected.

Let us consider two cases a) and b) (Fig.4.1)

Consider first the possible physical state of the node U and of the branch between the nodes U_i and U_j, which are represented by the values of the function F_i and f, i.e., case a). These values correspond to the given state of the conductivity. Let us try on the basis of the known values of F_i and f to deduce the value of the function F_j. Two possibilities exist in principle: the branch between the nodes U_i and U_j conduct, f = I, or the branch between the nodes U_i and U_j does not conduct, f = 0.

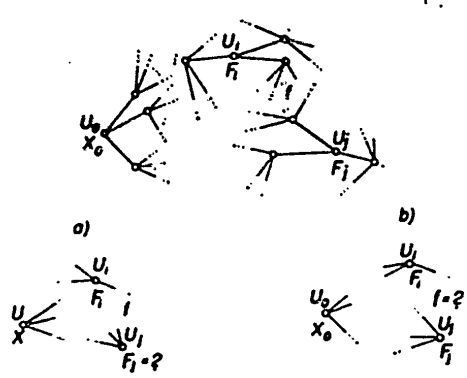

Fig.4.1

If the branch between the nodes conducts, f = I, then it depends on the physical state of the branch U_i. If the latter node is without voltage, $F_i = 0$, then the node U_j is also without voltage, so that $F_j = 0$. If the node U_i is under voltage, $F_i = I$, then the node U_j is also under voltage, $F_j = 1$.

In the second case the branch between the nodes U_i and U_j does not conduct, f = 0; if the node U_i is not under voltage, $F_j = 0$ then the second node is isolated from the node U_i, because the branch does not conduct, and we are unable to bring the problem to a logical conclusion, whether or not the node U_j is under voltage, and hence whether the function F_j = I or 0! If there is voltage in the node U_i,

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$F_i = I$, it cannot be in the node U_j, $F_j = 0$; if $F_j = 1$, then necessarily $f = I$*.

Next we carry out a somewhat different problem of a similar type. We assume that we know the values of the functions F_i and F_j, and we seek the value of the function f, i.e., case b). Also here, two possibilities exist in principle: the values of the functions F_i and F_j differ from each other (0, I; I, 0), or both values are the same (I, I; 0,0). This means, therefore, that in the first case there is voltage in the node but not in the other, or conversely, while in the second case there is voltage in both nodes or in neither.

In the first case we must have $f = 0$, because if this were not the case, i.e., if we had $f = I$, then the two nodes could be conductively connected, and $F_i = F_j = I$ would be valid; but this is contrary to the assumption from which we started.

The second case is more interesting: If $F_i = F_j = I$, then $f = I$** If we have for both nodes the value $F_i = F_j = 0$, then we are unable with the logical problem to ascertain the actual state of the conductivity of the branch between the nodes U_i and U_j, and hence we are unable to tell whether the branch does or does not conduct. Specifically, the value of the function j may be either 0 or I. Actually, if we have the value $f = 0$, then the two nodes are isolated from each other. According to the assumption neither of the nodes is under voltage. If $f = I$, then, of course, the nodes are connected, but since neither of them is under voltage, this state does not differ essentially from the preceding one.

---

* This non-symmetry of the value of the function F_j is due to the fact that we take into consideration only the input node. If the two nodes U_i and U_j were fed from two nodes (each with an independent source of the same voltage and polarity) then at $f = 0$ and $f_i = I$ it would be uncertain whether or not voltage was in the node U_j, i.e., $F_j = \sim$.

** When $F_i = I$ the node U_i is connected with the input U_0 as when $Fj = 1$; therefore, the two nodes U_i and U_j are connected via the input.

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From both cases it is seen that in the theory of switch circuits we encounter uncertainties, which manifest themselves in that we are unable to determine in some cases whether the branch does or does not conduct, or what value is assigned to the function in the particular node.

Let us consider cases a) and b) of Fig.4.1 differently. Suppose that we have to determine the unknown values of the functions F_i, f at the given values F_i, f in case a) and F_i, F_j in case b) in such a way that the I-subscheme with the value 0 is not connected with the subscheme with the value I. It is only in this way that we can determine the unknown values of the functions. In case a), therefore, we must enter in the 3rd line of the Table of Fig.4.2 the value F = ~, even though we know from the foregoing that F_j = 0 must be valid, which, however, does not contradict the previous finding that the value of the function F_j may be either 0 or I.

	F_i	f	F_j
1.	0	0	~
2.	0	1	0
3.	1	0	~
4.	1	1	1

Fig.4.2 – Table for Case of Uncertainty a)

x_1	x_2	x_3
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

F_i	f	F_j
0	0	~
1	1	1
1	0	~
0	1	0
1	0	~
0	1	0
0	0	~
1	1	1

Fig.4.3

In the first case a) we know the value of the function F_i in the node U_i and the value of the function f in the branch between the nodes U_i and U_j, and we seek the value of the function F_j. Four cases may occur.

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Analysis discloses in principle two cases: either f = I (cases 2 and 4) or f = O (cases 1 and 3). If f = I the I-subschemes are connected; if f = O the I-subschemes are disconnected. In the first case the values of the two functions F_i and F_j must be the same in order for the I-subschemes of different values to be disconnected. In the second case, because the nodes are disconnected, it does not depend on the value of the function F_j. In other words, the node U_j may lie in an I-subscheme to which is assigned either O or I. When the two I-subschemes are connected this does not occur through the branch with the function f. We explain in order to prepare the reader for the operation ω_1 described below. When we determine on this basis the value of the function in the node U_j we get the indefinite switch function F_j.

Example: Given the switch functions F_i and f in three variables, determine the function F_j.

Remarks: To the node U_j one of the 16 (2^4) definite functions which satisfy the indefinite function F_j may be assigned here.

With the indefinite function F_j occurring, three different values occur: O, I or ~. This gives rise to a new problem. Solve the given problem for the assumption that to the node U_i any indefinite function F_i is assigned. Given here are the values of the functions F_i and f, and we seek the value of F_j. The number of possibilities is increased, being six in all:

Take the 2nd and 5th lines. If we have the value of the function F_i = ~ , then the value of the function F_j may be anything depending on the value of the function f.

Now the problem of the second case b). Given the functions F_i and F_j in the nodes U_i and U_j, determine the value of the function f in such a way that the I-subschemes of different values are disconnected. If the value of the function f may be either I or O, we put it equal to ~ . Here again four cases exist (Fig.4.5)

Analysis of this case shows that in principle two cases may occur: either the

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values of the functions F_i and F_j are the same (lines 1 and 4) or they are different (lines 2 and 3). In the first case it is independent of the value of the function f, because the case cannot occur where I-subschemes are connected with f = 0

	F_i	f	F_j
1.	0	0	~
2.	~	0	~
3.	I	0	~
4.	0	I	0
5.	~	I	~
6.	I	I	I

Fig.4.4

	F_i	f	F_j
1.	0	~	0
2.	0	0	I
3.	I	0	0
4.	I	~	I

Fig.4.5 – Table for Case of Uncertainty b)

or I. In the second case we must have the value f = 0 in order to satisfy the given condition. Therefore, we get the indefinite function f. If the functions assigned to the nodes U_i and U_j are indefinite, we get a larger number of possibilities. This case is discussed in part 5.2.

The two cases a) and b) just discussed illustrate sufficiently the occurrence of indefinite switch functions. The possibility of their employment has been investigated on an elementary problem, i.e., the prevention of the connection of two I-subschemes with two different definite values. In both cases the indefinite functions were determined in advance for forming the basis for the two fundamental operations of the method, which we call ω_1 and ω_2.

5. Method

5.1 Operation ω_1. We have to construct any function F, $\{0\} \neq \{F\} \neq \{I\}$ in a definite node in a scheme. As already stated in part 2, it is shown how to construct such a scheme in which the node U lies in such a way that every value I of the function lies in the I-subscheme which includes the input pole, and no value 0 of the function F lies in the I-subscheme which includes the input pole, and, in the event

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that the indefinite value ~ is permissible, we may select one of the two above-mentioned possibilities which seems the better able to fulfull the conditions of the construction of the function F.

As already stated, the construction of the function of the function starts with the node U. According to the assumption that the function F contains at least one value I, so that for the construction of the function F we have to start with a node U at least one Σ-branch (Fig.5.1). The value of the function F and the value of some function f of the Σ-branch are therefore given; we have to determine the value of the function F_1 in the second node of the Σ-branch in such a way that the function F can be constructed with the help of the function F_1.

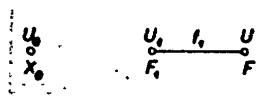

Fig.5.1

	F_1	f	F
1.	~	0	0
2.	~	0	~
3.	~	0	I
4.	0	I	0
5.	~	I	~
6.	I	I	I

Fig.5.2

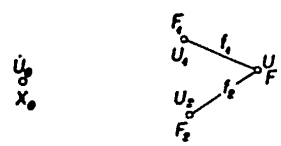

Fig.5.3

Example: If, for a definite combination of the values of the argument F = I is valid, we have the value of the function f = I, then it is possible to construct the value of the function F_1 = I, and hence also the value I of the function F.

It should be noted that the problem is formulated here somewhat differently than in part 4, in which the occurrence of indefinite functions is discussed. Part 4 is concerned only with the determination of the functions in such a way that the I-subscheme with the value 0 is not connected with the I-subscheme with the value I.

The Table of Fig.5.2 is constructed exactly like the preceding Tables. Let us

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examine more closely the case in which we have the value of the function F = I. There are two: the first at f = 0 in the 3rd line and the second at f = I in the 6th line. We see that in the 6th line we can with the help of the Σ-branch construct the value I of the function F. In the case of the 3rd line, however, we are unable to fulfill the conditions of the construction because f = 0. In this case the value of the function F_1 may, of course, be a ~, but, even if the value were changed to I, the voltage could not for this state go via the Σ-branch to the node U. We assume, of course, that only one Σ-branch starts at the node U. In the case of line 3 we must further find one or more Σ-branches with such a function that at least one of the values of the function of the Σ-branch is I.

Operation ω_1 is called the analysis of the switch function F in the node U, or, briefly, the analysis of the function F. The analysis is called complete if for each of the 2^n states of the conductivity for which F = I is valid, there exists at least one Σ-branch with such a U that its function f = I. As long as at least one I of the function F for which the statement condition is not fulfilled exists, we speak of an incomplete analysis. When an analysis is such that a further Σ-branch is complete it will be called a superfluous analysis and the branch a superfluous Σ-branch. Operation ω_1 will always be carried out with only one Σ-branch, whether or not the analysis is complete. With this operation, therefore, one new node is formed.

Remark: By analysis alone, the condition of the construction of function cannot be fulfilled. This condition, i.e., the connection of the actual input pole with the node U, is first carried out in the second operation ω_2.

The examples of Fig.5.3 and 5.4 are concerned with the complete analysis of the function F. We see that for a complete analysis neither the function f_1 nor the function f_2 alone is sufficient. Only both functions enable a complete analysis. If the analysis is carried out only with the help of the function f_1, the conditions of a complete analysis of the 5th line of the Table are not fulfilled.

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Take the 6th line of the Table as an example. The value of the function F is I, and both values of the functions f_1 and f_2 are equal to I, so that we also have for both values of the function $F_{1,2}$ = I. In other words, we have two possibilities for fulfilling the requirements for the construction of the function F: either with the help of the function F_1 or with the help of the function F_2. The definite values of the functions F and $F_{1,2}$ in this case are donated somewhat differently, i.e., by writing not unity I but unity 1. The latter value is called conditional unity.

	F_1	f_1	F	f_2	F_2	x_1	x_2	x_3
1.	~	0	0	0	~	0	0	0
2.	I	I	I	0	~	0	0	I
3.	~	0	0	0	~	0	I	0
4.	0	I	0	0	~	0	I	I
5.	~	0	I	I	I	I	0	0
6.	I,1	I	I,1	I	I,1	I	0	I
7.	~	0	~	I	~	I	I	0
8.	~	I	~	I	~	I	I	I

Fig.5.4

Following are some further important concepts: 1. The node $U_{1,2}$, when formed by the analysis, is called the front node. What is concerned here is a complete analysis with the following characteristic: if its function is constructed, its function F is also automatically constructed. In every stage of the solution the set of the front node P must have this characteristic (instead of the function F, therefore, the prescribed function X_k, k = 1, 2, ..., m is valid). The rest of the nodes in the scheme are called back nodes (the nodes U_0 and U in the example of Fig.5.3).

2. If the condition of the construction of the definite I has been fulfilled, it is advisable to denote this in some way on the I-subscheme, in order not to try to fulfill some condition. This can be done by the introduction of one more value of I, i.e., 1. When this value appears in a function it means that the function is

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already constructed.

Remark: The value 1 is defined with the help of the front nodes, where the value 1 lies in an I-subscheme including a number greater than 1 of front nodes.

Finally, we now can construct the complete Table for the analysis of the function F and formulate clearly the procedure for carrying out this operation.

Condition for Operation ε_1: The analysis is carried out in the front node U whose function has at least one value I and at least one value O.

Remark: If the function F does not have any value O, the analysis would in this case be superfluous and indefinite, because the node U, as will be seen later,

Table for operation ω_1

F	T
0	0
~	~
I	I
I	I
I	~

Fig.5.5

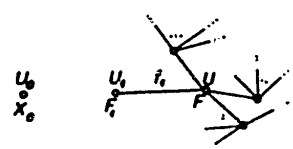

Fig.5.6

is in this case connected with the input pole of operation ω_2. If the function F does not have any value I, there is nothing to construct.

Purpose of Operation ω_1: The purpose of this operation is to find an node whose function does not contain the value O. It is only by analysis that new intermediate nodes with an indefinite function occur in the scheme, which usually have a larger number of indefinite values than the analyzed functions.

The function Σ-branch f_1, which participates in the analysis, must be selected somehow. Therefore we determine in advance for the given function F the value of the auxiliary function φ. This function constitutes the reference for the selection of the function f_1. The value of the function φ is prescribed wholly arbitrarily. Specifically, it is not necessary to use all of the values of the function φ, and

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usually this is not done. However, the larger the number of zeros which are used, the smaller is the number of zeros in the function F_1 (Fig.5.7). The larger the number of unities which is used, the larger must be the number of unities to construct with the help of the node U_1.

F	f_1	F_1
0	0	~
~	0	~
(I) I	0	~
I	0	~
I	0	~
~	I	0
(I) I	I	I (I)
(I) I	I	I (I)
I	I	I

Fig.5.7 - Table for Determination of Function F_1

It should also be mentioned that a new node U_1 is always introduced. The function f of the Σ-branch, with whose help the new node is introduced, may be any function of the Σ -branch. This also follows from Fig.5.7, because for every combination of values of the functions F and f_1, we introduce a definite value of the function F_1. However, not all of the functions f are equally good from the viewpoint of the economy of the solution which we are seeking, as has already been mentioned above. The value of the function φ for the value of the function F is constructed as follows:

If f = 0 it is good for the value φ to be zero, because this enables us to permit the value F_1 = ~ ;

If F = ~ , it does not depend on the value of the function φ ;

If F = I,1 it is good for the value of φ to be 1, because this enables us to construct I of the function F;

If F = 1, it can be constructed backward in one way or another (with the help of the Σ -branch starting at the node U), see Fig.5.6, because it is independent of the function φ.

After we have selected according to φ the function f_1, we determine with the help of the functions F and f_1 the function F_1 according to the accompanying Table. The meanings of the values enclosed in parenthesis will be understood from the

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following paragraph.

Remark: If the function F_1 does not contain 0, the node U_1 can be connected directly with the input node. However, usually this is not done.

Execution of Operation ω_1: First we determined for the function F the function f_1 of the Σ-branch necessary in the form of the indefinite function φ. For this indefinite function we select any function f_1 from the set of functions ω of the Σ-branch.

Result of Analysis: The result of the analysis is a new front node U_1 with function F_1 connected via the Σ-branch with the function f_1 of the node U whose function F has been analyzed.

Two possible cases exist: either the node U must or must not remain in the set of front nodes in order for this set to have the necessary characteristics, i.e., the analysis is either incomplete or complete. In the first case both nodes are front nodes after the operation, in the second case one of the front nodes U is abolished by the operation and the front node U_1 is formed.

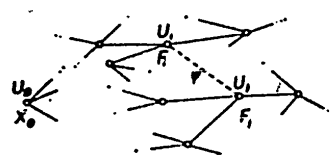

Fig.5.8

The meaning of the values enclosed in parentheses in Fig.5.7 is as follows. In order for the condition for the values 1 and I to be satisfied with respect to the front nodes, we usually must carry out after the operation the substitution of some value 1 → I or I → 1.

5.2 Operation ω_2. In the preceding part 5.1, we have seen that it is useful to introduce two further values, i.e., 1 and 1, besides the fundamental values 0, ~, and I. At the operation, therefore, we must reckon with five values. For the considered purpose of the operation, however, it is not good to operate immediately with the five value. This would be unmanageable; therefore we shall explain the

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principle of the operation with reference to the three fundamental values.

Assume that we are constructing a scheme, and are in the stage represented in Fig.5.8. The scheme is wholly independent of the structure, and all that is essential is that the nodes U_i and U_j are front nodes and that their functions contain only the three types of values: 0, I and ~ . Between the nodes is some branch with the function f^n. (This state can be obtained by the actual solution if no unity I has yet been constructed by abolishing the value 1 and putting I for it.)

As already explained in part 4, the basis of the operation is the finding of the function of the branch which may be permitted between the two given nodes.

We have then the two nodes U_i and U_j with the functions F_i and F_j (Fig.5.8), and, as was also the case with operation ω_1, we try to determine the conditions for the function f of the branch connecting the two nodes in the form of the auxiliary indefinite function ψ . Here the determination of the function will not be complicated by the fact that some branch with the function f^n is already present between the nodes. Specifically, between the two given nodes, a whole series of difference branches with the function $f_p(x_1, x_2, \ldots, x_n)$ may be present; this follows from the indefiniteness of the problem of determining for the two given functions F_i and F_j the function f of the branch connecting the corresponding nodes (see above). The uncertainty is due to the fact that two branches exist whose functions for the considered value of the argument have the values $f_{p1} = 0$ and $f_{p2} = I$. From this it clearly follows that for this value of the argument there can be a value of the auxiliary function $\psi = \sim$. This, however, can be determined in advance without actually having all of the possible functions f_p permissible for the branch between the nodes, i.e., by putting $\psi = \sim$ for the value of the auxiliary function in this case. This can be determined on the basis of the values of the functions F_i and F_j.

The Table of Fig.5.9 is constructed wholly analogously to the Tables of part 4. It will be noted that in its last line we have the value $F_{i,j} = I$ and the

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value $\psi = \sim$. It is wholly clear that the scheme becomes correct, i.e., without gaps, if the value of the function f is either 0 or I. If, however, we have succeeded in connecting the I-subschemes of the value I of the functions f_i and F_j,

F_i	ψ	F_j
•	~	0
•	~	~
•	~	I
~	~	•
~	•	~
~	~	I
I	~	0
I	~	~
I	~	I

Fig.5.9 – Table for Determination of Function

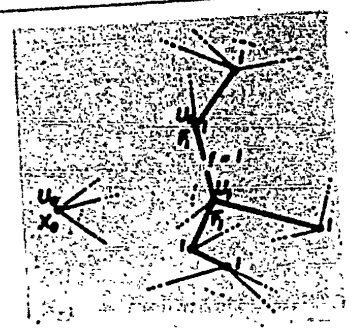

Fig.5.10

so that we have the value f = I, then we have two possible results. It depends on the state present before the operation, i.e., on whether or not the I-subschemes were connected, so that we had or did not have f'' = I, before carrying out the operation. In the first case no further connections can be obtained. In the second case two possibilities for the construction of the I on these I-subschemes arise directly, either by means of the function of the front node U_i or by means of the function of the front node U_j. As soon as f = I we can put for all of the functions on the I-subschemes the value 1.. The value 1 occurs not only at analysis ω_1 but also at operation ω_2. This case is represented in Fig.5.10. The Σ-branches where f = I are denoted by heavy lines.

The connection of the I-subschemes is obtained by adding the Σ-branch whose function f = I, because f'' = 0. The function f must satisfy the function ψ, otherwise a gap occurs. Two possibilities exist here: either the function f of the Σ-branch with the value I for the given state which satisfies the function ψ exists or it does not exist. In the first case it is possible to connect the two

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I-subschemes with the Σ-branch, while in the second case it is not possible to do so. We assume, of course, that for the construction of the schemes, elements more complicated than Σ-branches are not employed.

From the case just analyzed we see one of the possibilities which may be useful at operation ω_2 for many solutions: to increase the number of alternatives with whose help the value I can be constructed.

Another possibility is: by connecting the I-subscheme with the value I or 1 with the I-subscheme with the value 1, it is actually possible to construct the values I and 1.

A still further possibility consist in that when Ψ does not contain 0 it is permissible to connect the nodes U_i and U_j directly with each other. All of the possibilities occurring are described in detail at the end of the description of operation ω_2. As an example, if one of the nodes U_i or U_j is before the operation a front node and the operations on the two nodes flow together so that one node U is formed, then one of the front nodes is abolished with the help of the operation, which is advantageous for the solution.

We are now able to construct the complete Table for operation ω_2 and formulate clearly the procedure for carrying out this operation. By the introduction of the two further values 1,1 we get a further series of possibilities for the problem of connections, but the construction of the Table is similar except for the employment of these further values.

Conditions for Operation ω_2: The operation is carried out on the nodes U_i and U_j only if at least one of them is a front node. The operation can be carried out only when a Σ-branch which satisfies the indefinite function Ψ exists.

Remark: Operation ω_2, even when it can be carried out, is not always advantageous. The class of less-advantageous operations is described in detail at the end of the description of operation ω_2.

Purpose of Operation ω_2: The purpose of operation ω_2 is, among other things,

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to increase the number of nodes with whose help the value 1 or I can be constructed, or to construct these values directly. This also includes the special but important case where the function F in the particular front node U does not contain the value 0. Its comparison with the function of the input pole (which is equal to 1 at all of the functional places) follows from the fact that (f) can be (I) and the node U can be connected with the input pole. Moreover, with this operation we can abolish either or both of two front nodes. Sometimes it occurs by direct connection

	a)			b)		
	F_i	F_j	Ψ	f	F_i	F_j
0.1	0	0	~	0 I	0	0
0.2	~	0	~	0 I	~	0
0.3	I	0	0	0	I	0
0.4	I	0	0	0	I	0
0.5	I	0	0	0	I	0
1.1	~	~	~	0 I	~	~
1.2	I	~	~	0 I	I(I)	~ I(I)
1.3	I	~	~	0 I	I(I)	~ I(I)
1.4	I	~	~	0 I	I	~ I
2.2	I	I	~; I	0 I	I(I)	I(I)
2.3	I	I	I	0 I	I I(I)	I I(I)
2.4	I	I	I	0 I	I	I I
3.3	I	I	~; I	0 I	I(I)	I(I)
3.4	I	I	I	0 I	I	I I
4.4	I	I	~	0 I	I	I

Fig.5.11 -

Table for Determining the Auxiliary Function Ψ for Operation ω_2

a) Before operation; b) After operation

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of the nodes U_i and U_j when the node U is formed whose function is nearly the same as F_i or F_j, which is likewise advantageous.

Table for Operation ω_2: The Table of Fig.5.11 contains all of the possible combinations of the five value 0, ~ , I, I and 1. For each of the combinations, the value fo the auxiliary indefinite function Ψ to be applied to the function f for correction of the function F_i and F_j is given.

Remark: There are in all 25 combinations of the five functional values. These combinations were numbered in the manner which can be seen from the first five lines of the Table. Because 10 lines of the Table are superfluous (regardless of the sequence of the combinations) these lines were left out. The numbering is left in the original form.

In cases 2.2 and 3.3 we require for Ψ the value ~ if the values of both functions F_i and F_j lie on one I-subscheme or the value 1 if they lie on I-subschemes. We see at once that in the first case it is unnecessary to connect another I-subscheme, while in the second case this is usually useful.

Procedure for Operation ω_2: On the basis of the functions F_i and F_j we determine the functional value of the auxiliary indefinite function Ψ. Its value is prescribed in such a way that no gaps occur. For the indefinite function Ψ, we find the definite function f. If several functions $f_1, f_2, \ldots, f_p$ which satisfy the function Ψ exist, we take the one which is the most advantageous according to our investigation. If we denote the number of the indefinite places of the function Ψ u and the number of places with the value lv, then the indefinite functions Ψ satisfy 2^{u+v} definite functions. It may happen that not one of these functions occurs among the functions f of the Σ-branch. In this case we proceed to another pair of nodes. If such a function f which satisfied the auxiliar function Ψ exists, we ascertain whether we can connect the Σ-branch. If the operation is carried out advantageously (see the purpose of operation ω_2) the Σ-branch [illegible] and if not the Σ-branch is not connected and we proceed with another

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operation. If we connect the Σ-branch we determine for it the values of the functions F_i and F_j according to the Table. The values I and 1 of the functions F_i and F_j can be further corrected according to the results of the respective operations with respect to the front nodes. That is, where there is in the function the value I and I-subscheme in which the values lie must include just one front node and the value 1 at least two. The operation may take in either the node U_i or the node U_j or both nodes, or some other node of the set of back nodes. The possible results of the operations are clearly analyzed in the next paragraph.

Results of Operation ω_2: The results of the operations are classified with respect to the front nodes and with respect to the function {f} with whose help the operation is carried out. {f} may be either {I} or ≠ {I}. Four possibilities occur: before the operation either both nodes are front nodes or only one of them is a front node; in both cases the function {f} may be either {I} or ≠ {I}. Let us now analyze these possibilities.

1. Both nodes U_i and U_j are front nodes before the operation.

1.1 The function {f} ≠ {I}. The resultant node is denoted U and its function F. Two cases can occur: either the node must be in the set P, a front node in order for this set to have the necessary characteristic, or it must not do so. This set must have the following characteristic: if we construct the functions of its nodes, we likewise construct the function of the output pole. In the first case one of the front nodes is abolished, leaving the front node U, in the second, the two front nodes U_i and U_j are abolished and formed the back node U.

1.2 The function {f} ≠ {I}. Three cases may occur in principle. They are again classified from the viewpoint of whether the nodes U_i and U_j in the set must or must not be front nodes*. Both of them go to the back nodes, or either of them, or neither of them.

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* In some cases we can select the nodes to be included in the set P.

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2. Before the operation, the node U_i is a front node and the node U_j a back node:

2.1 The function $\{f\} = \{I\}$. The resultant node goes to the set of back nodes only if it satisfies the condition prescribed for the set P. Otherwise it does not do so.

2.2 The function $\{f\} \neq \{I\}$. The node U_i goes to the set of back nodes only if it satisfies the condition prescribed for the front nodes.

Remark: It seems that at the construction of the schemes we can proceed in such a way that the constructed scheme does not have superfluous switch elements (after removal of such elements the scheme is correct, i.e., without negative or positive gaps).

If, however, operation ω_2 is carried out without limit such a scheme is not obtained. Sometimes operation ω_2 forms superfluous switch elements in the scheme. We have afterward two possibilities: either to carry out the operation, but afterward to abolish the superfluous switch elements, or not to carry out the operation and carry out another operation.

If the solution is carried out by a human being, everything that he has to do is not prescribed. Much depends on the whole situation at the solution. In planning the solution for the machine, it is perhaps better to refrain from abolishing the superfluous elements of the scheme for the sake of the simplicity of the procedure.

However, the detailed analysis of the method for the solution from this viewpoint is a part of the further development necessary for the machines. This cannot be undertaken in the present article. We limit ourselves here to an example of such an operation ω_2 carried out on a loop scheme.

Example: Carry out operation ω_2 for the direct connection of two nodes sometimes conducting in the loop scheme represented in Fig.5.12. If the scheme S does not connect a front node or pole, the loop scheme is without sense. This is so

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because the voltage can get into the loop only via the node U, and because in the loop there is no front node or pole closing by means of a loop of any I-subscheme for the construction of some unit of the output pole. Figure 5.13 likewise represents an example of such a loop. The loop was formed as follows: In node U, the

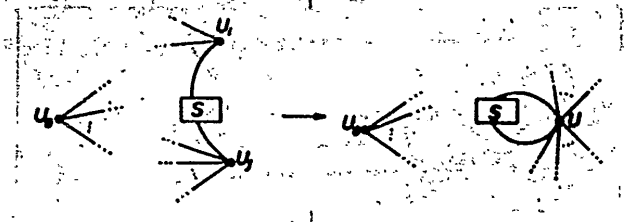
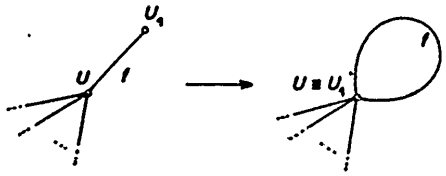


Fig.5.12 - Formation of Loop

analysis of the function F of the Σ-branch with the function f was carried out. The node U_1 was formed. By the subsequent operation ω_2 we can connect the nodes U and U_1, which conducts to the loop.



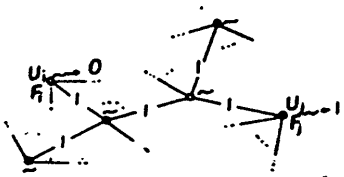


Fig.5.13 - Example of Formation of Loop

Fig.5.14

5.3 Operation ω_3. Finally, we describe th third operation, which has an auxiliary but important significance. It follows from the example. We have the definite I-subscheme with the value ~ (Fig.5.14).

We carry out in the node U_1 on the function F_1, the operation by which its value ~ is changed to zero. If 0 is not substituted for the value ~ over the

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whole I-subscheme, then, at further operation on the function F_j it must change from the value ~ to I. If we carry out this change we get oversound. Physically, this means that for the particular state of switch circuit, voltage is obtained in the node U_j and hence also unto the node U_i, but the latter is oversound. At the construction of the scheme, therefore, we must observe the following rule: In any I-subscheme there must always be only one of the five values: 0, I, 1, ~ or 1.

	a)		b)
	φ	ψ	
0	c)	d)	e)
~	f)		g)
I	h)		i)
1			j)
1			k)

Fig.5.15

a) Auxiliary values of functions φ, ψ for selection of function f; b) Auxiliary value of function in node; c) Recommended that value of function f of Σ-branch be 0; d) Value of function of Σ-branch must be 0, otherwise operation cannot be carried out; e) Value of function must be 0, otherwise oversound occurs; f) Value of function f may be 0 or I; g) Value of function may be 0, 1, I or 1; h) Recommended but not absolutely necessary that value of function f be equal to 1; i) Value lies in I-subscheme which includes at least two front nodes; j) Value lies in I-subscheme including just one front node; k) Value lies in I-subscheme including input pole

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Usually during operation ω_1 or ω_2, the situation in the scheme changes fairly much. During the construction of a scheme in one I-subscheme, a series of functional values may alternate at a particular function place in the function in the node. Following are typical sequences:

1. ~ , 0

2. ~, I, 1, I, 1, 1.

In case 1 the value ~ changes at the first operation to 0. In case 2 the value ~ is changed by the first operation to I, then the number of possibilities of constructing the value (1) is increased and by several operations to change to (I), and, finally, by again increasing (1), of constructing the value (1).

It is seen from the foregoing that the values 0 and 1 are stable and further unchanged, while the values I and 1 can change into each other. For the value ~ one of the values 0, 1, I, and 1 must be substituted.

All of the possible auxiliary values and their significance are presented in Table of Fig.5.15 below.

From the Table and the text it can be seen that the values 1, ~ and as employed here are not functional values in the normal sense of the word, but are auxiliary values, which can be conveniently employed for the whole development of the construction of the scheme, and at all of the alternatives which occur.

5.4 Procedure for Construction of Scheme. We can now proceed with the description of the procedure for the solution. According to what has been said above, it is wholly logical to begin the construction of the scheme with the output poles.

In the initial stage we have in the scheme several output poles, which are front poles, and one input pole, which is a back pole.

From this point we have a number of possibilities of how to proceed further. At the first operation what is concerned is which of the functions to analyze, and at the second operation ω_2 which pair of nodes to select. Here fundamental difficulties are encountered, some of which occur with all of the known methods. It is

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advantageous to begin with operation ω_2, because this operation does not increase the number of intermediate nodes. The solution of the penetration can sometimes be accelerated in the initial stage of this operation. The operations are then alternated according to the development of the scheme and the number of Σ-branches and nodes in the scheme.

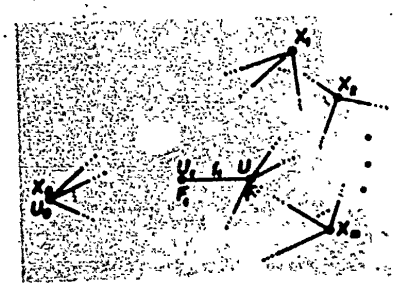

Fig.5.16

Assume that we are in the ith stage of the solution. In the scheme there is some set of front nodes P and some set of back nodes Z. In this stage we begin with the analysis of the switch function in one of the front nodes, for example U (Fig.5.16). The Σ-branch f_1 is analyzed there. Next it is advantageous to try to carry out operation ω_2 with one of the pair of nodes U_1 and U_0 or some other nodes in the scheme. Next we carried out wholly analogously analysis either in the node U, if it is a front node, or in another front node, provided any front nodes are present in the scheme. When no front nodes are present, we are finished.

If the solution is carried out by a man, he stops after a length of time because he has to be economical (see example in part 6). We are not able to mention here all of the operations with whose help the solution can be constructed, because this would be interminable, but it should be noted that such a sequence of operations always exists. For the machine, however, it is necessary to determine for the operations ω_1 and ω_2 the conditions at whose satisfaction the solution is definitive. The determination of these conditions is a partial problem of the detailed analysis of the process of solution of the problem for the machine. The whole analysis will be the subject of a future article.

6. Examples

For illustrating the application of the method, we present two fairly simple

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examples. The examples were selected at random. From this it follows that the solution will not necessarily be the most advantageous one. Moreover, it is not the purpose of the examples to give the most advantageous solutions. It may be that

x_1	x_2	X
0	0	1
0	1	0
1	0	0
1	1	1

Fig.6.1

x_1	$\bar{x}_1$	x_2	$\bar{x}_2$
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0

Fig.6.2

the reader after a little experience can find a better solution.

1. We have the operational Table of the scheme in Fig.6.1.

This example is so simple that a particular method is unnecessary for its solution, because the solution follows directly from the Table. It is merely given for facilitating the reader's understanding of the method.

F_1			F_2		
F_1^1	F_1^2	. . .	F_2^1	F_2^2	. . .

Fig.6.3 - Form for Formation of Function F_i^j

n	j
2	3
3	6
4	8
5	10

Fig.6.4

We describe first the expedients used for the solution and then the actual solution of the problem.

The function f of the Σ-branch is composed of the four fundamental functions* represented in Fig.6.2, and which can be formed with the help of paper strips.

As already mentioned, we can form 8 (i.e., $3^2 - 1$) different Σ-branches:

* At n variables we have available $2n$ fundamental functions.

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x_1, $\bar{x}_1$, x_2, $x_2 + x_1$, $x_2 + \bar{x}_1$, $\bar{x}_2$, $\bar{x}_2 + x_1$, and $\bar{x}_2 + \bar{x}_1$.

At a larger number of variables it is usually impossible to survey all of the Σ-branches. In this case a little investigation is sufficient for deciding in the given case which of the fundamental functions must be included in the functions of the Σ-branches. We put down not only the fundamental functions themselves, but also their sum f = I, if at least one of the fundamental functions equals I. The auxiliary functions, for example, φ and ψ are advantageously noted on paper stripe. For

X_0	X			F_1		F_2	
	X^1	X^2	X^3	F_1^1	F_1^2	F_2^1	F_2^2
1	1	1	1	~	~	1	1
1	0	0	0	0	0	0	0
1	0	0	0	I	I	~	1
1	I	1	1	I	1	~	~

ψ_0	ψ_1	ψ_2	f_2	ψ_3	ψ_4	f_4	ψ_5	f_5	φ_5	f_5
1	~	~	0	~	1	1	1	0	1	I
0	~	0	0	~	0	0	0	1	0	1
0	~	~	1	~	~	I	0	0	0	0
1	~	1	1	~	~	0	1	I	1	0

Fig.6.5

the solution another form is required, which is represented in Fig.6.3. In the form we enter the successive forms of the function F in the nodes. This is necessary, on the one hand, because after each operation some of the values of some of the functions are changed, and, on the other, for the survey we must know the successive stages of the functions; this is also necessary for verifying whether the scheme actually developed without oversounds. That is, the momentary oversounds are listed in the Table. The symbol F_i^j in the Table denotes the jth form of the ith function F_i in the node. For a whole series of cases it is sufficient to select j according to Fig.6.4.

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Room for drawing the scheme is also necessary.

The method of solution depends much on the successive stages reached at the solution. It would be ideal if all of the successive stages could be represented. This, however, is technically impossible. Therefore, the reader who wishes to familiarize himself with the method should form the four fundamental functions of Fig.6.2 in the form of strips of stiff paper and the form for the forms of the functions of Fig.6.4.

Fig.6.6

In the initial stage of the solution, we have on the scheme the input pole U_0 with the function X_0 and the output pole U with the function X^1. Both forms of the function are entered in the Table of Fig.6.5. For survey the auxiliary functions φ and ψ and the functions of the selected Σ-branch of Fig.6.5 are also represented.

As the first operation we may carry out either the analysis or operation ω_2. Let us try to carry out operation ω_2. Therefore we determine for the functions X_0 and X^1 the indefinite function ψ_0 according to the rule given in part 5.2. From the nature of the function f of the Σ-branch, it follows that the operation cannot be carried out, because none of the functions equals 0 for the 2nd and 3rd lines (Fig.6.2). Therefore, we proceed to the analysis of the function X^1.

Next we determine for the function X^1 the indefinite function φ_1. From the set of Σ-branches it follows that we can carry out the analysis with the help of a whole series of Σ-branches. It happens that in this simple example it makes no difference whatever one of the possibilities is selected. Suppose that we select $f_1 = x_2$. The node is connected at one node with the output pole and the other node forms the first intermediate node, see Fig.6.6. With this the analysis is not complete. We therefore carry out another operation ω_1. For the indefinite function φ_2 we select the function $f_2 = \bar{x}_1$. This completes the analysis. Next we also connect

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this Σ-branch like the preceding Σ-branch. With the newly-formed front nodes we get the forms of the functions F_1^1 and F_2^1.

Next let us try to carry out some connection with the help of operation ω_2. Both functions $F_{1,2}^1$ contain 0, so that their respective nodes cannot be directly connected with the input pole. Of the three possibilities of the connection of some pair of nodes with the functions F_1^1, F_2^1 and X^1, two of the possibilities (the connections F_1^1, X^1 and F_2^1, X^1) lead to a loop, and the third possibility although realizable (i.e., the auxiliary function ψ_1) leads to a parallel connection of the two Σ-branches. The formed scheme would be equivalent to the scheme obtained by the preceding analysis of the function X^1 with the help of the Σ-branch $f = x_2 + \bar{x}_1$.

x_1	x_2	x_3		X_1	X_2	X_3
0	0	0		0	1	0
0	0	1		1	~	1
0	1	0		0	0	1
0	1	1		1	1	0
1	0	0		0	1	~
1	0	1		1	1	1
1	1	0		0	~	0
1	1	1		0	0	0

Fig.6.7

Let us turn to the function F_1^1. Let us try to connect this node with the input pole of the Σ-branch. The indefinite function ψ_2 satisfies the function $f_3 = x_1$. The Σ-branch with the function f_3 is connected because the function ψ_2 is fully satisfied. The new forms of the functions F_1^2, X^2 are formed.

We have succeeded in constructing one unit of the function X. In the scheme a front node remains with the function F_2^1. Concerning the connection of the nodes with the functions F_1^2 and F_2^1, it is again valid that although the connection is realizable (i.e., with the auxiliary function ψ_3) it leads to a parallel connection of the two Σ-branches.

However, in exactly the same way as at the preceding operation, the connection of the nodes with the functions F_2^1 and X_0 can be carried out. The indefinite function ψ_4 satisfies $f_4 = \bar{x}_3$. The new forms of the functions F_2^2 and X^3 are formed.

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Because all of the values I of the function X are constructed, the solution is complete.

2. The second example is a little more complicated. We have the operational Table of Fig.6.7. The function $X_{1,2,3}$ is denoted the initial stage $X^1_{1,2,3}$, and we enter it together with the function of the input pole X_0 in the Table of Fig.6.8.

In the initial stage we have in the scheme four poles: one input pole and three output poles. Let us try the first operation ω_2. The condition for the connection of the nodes X^1_2 and X^1_3 is determined in the form of the indefinite function ψ_1. However, not much would be gained by the connection of the nodes, so we proceed to another pair. For the pair of nodes X^1_1 and X^1_2 we determine the indefinite function ψ_2. This function satisfies $f_1 = x_3$. The connection seems fairly good, because two of the values I of each of the functions X^1_1 and X^1_2 change to the values 1, so that we carried it out. Two new forms of the functions X^2_1 and X^2_2 are formed. The third possibility remains to be tried, i.e., the connection of the nodes X^2_1 and X^1_3. The indefinite function ψ_3 satisfies the function $f_2 = \bar{x}_2$. The connection seems good, because again some values I change to 1. The new forms of the functions X^3_1, X^2_3, X^3_2 are formed.

This is the initial stage, and next we proceed to the analysis of one of the functions X^3_1, X^3_2, X^2_3. The nodes corresponding to these functions are front nodes. We take, for example, X^3_2. The function φ_1 satisfies fairly well $f_3 = \bar{x}_2$. One of the values 1 is not constructed by the analyzed, but this is wholly inconsequential.

We get a front node with the function F^1_1. In comparing the function F^1_1 with the function X_0 we see that one of them corresponds to a connected node. The form: $F^2_1 = X_0$, X^4_1, X^4_2, X^4_3 occurs. The node with the function X^4_2 goes over to the set Z. Next we analyze the function X^4_1. The function φ_2 satisfies very well the function $f_4 = x_3$. A new front node arises with the function F^1_2. The node with the function X^4_1 goes over to the set Z. F^1_2 contains 0, so that the node is not connected with the input. Next we ascertain the possibility of carrying out operation ω_2.

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Connection of the nodes with the functions X_1^4 and F_2^1 is excluded. It would also be senseless to connect the node with the function F_2^1 and the nodes with the functions X_2^4 and X_3^3. Instead of operation ω_2 therefore it is better to try analysis with

	X_1	X_2	X_3	F_1	F_2	F_3	F_4
X_0	$X_1^1 X_1^2 X_1^3 X_1^4 X_1^5$	$X_2^1 X_2^2 X_2^3 X_2^4 X_2^5$	$X_3^1 X_3^2 X_3^3 X_3^4$	$F_1^1 F_1^2$	$F_2^1 F_2^2 F_2^3$	$F_3^1 F_3^2$	$F_4^1 F_4^2$
1	0 0 0 0 0	1 1 1 1 1	0 0 0 0	1 1	~ 1 1	~ 1	~ 1
1	1 1 1 1 1	~ 1 1 1 1	1 1 1 1	1 1	1 1 1	~ 1	~ ~
1	0 0 0 0 0	0 0 0 0 0	1 1 1 1	~ 1	~ 1 1	~ 1	1 1
1	1 1 1 1 1	1 1 1 1 1	0 0 0 0	~ 1	1 1 1	1 1	0 0
1	0 0 0 0 0	1 1 1 1 1	~ 0 0 0	1 1	~ ~ ~	~ 1	~ ~
1	1 1 1 1 1	1 1 1 1 1	1 1 1 1	1 1	1 1 1	~ 1	~ ~
1	0 0 0 0 0	~ 0 0 0 0	0 0 0 0	~ 1	~ ~ 0	~ 1	0 0
1	0 0 0 0 0	0 0 0 0 0	0 0 0 0	~ 1	0 0 0	~ 1	0 0

φ_1	φ_2	f_1	φ_3	f_2	φ_4	φ_5	f_3	φ_1	f_3	φ_2	f_4	φ_3	f_4	φ_4	f_4
0	0	0	~	1	0	~	1	1	1	0	0	~	1	0	0
~	~	1	1	1	~	~	0	1	1	~	1	~	1	~	0
0	~	0	0	0	1	1	1	0	0	0	0	~	1	1	1
0	1	1	0	0	0	0	0	1	0	1	1	1	1	0	1
~	0	0	~	1	~	~	1	1	1	0	0	~	0	0	0
1	1	1	1	1	~	~	0	1	1	~	1	~	0	~	0
~	~	0	~	0	~	~	1	0	0	0	0	~	0	0	1
0	1	1	~	0	~	~	0	0	0	0	1	0	0	0	1

Fig.6.8

operation ω_1. The function F_2^1 is again advantageously analyzed, because by it we obtain three front nodes with the functions F_2^1, X_1^4, X_2^4. The indefinite function φ_3 satisfies $f_5 = \bar{x}_1$. We get the forms F_2^2, X_1^5, X_2^5. One of the nodes X_3^3 remains to be determined. The connection of the node with the remaining nodes in the scheme would be wholly senseless, so that we analyze its function. If we want to connect, for example, the nodes with the functions F_2^2 and X_3^3, we find that the indefinite function φ_4 does not satisfy any of the functions f of the Σ-branches. The function φ_4 satisfies $f_6 = x_2$. However, here again the new node F_4^1 is not connected with the

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input. We again try its connection with F_2^2. The function W_5 satisfies $f_7 = \bar{x}_3$. We get the forms F_2^3, F_4^2, I_3^4, and with this the solution is carried out. Its relay scheme is represented in Fig.6.10.

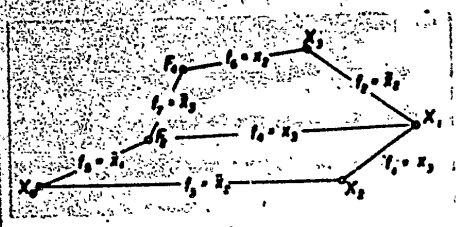

Fig.6.9

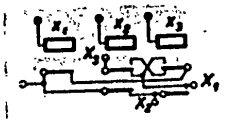

Fig.6.10 – Relay Scheme of Circuit Represented in Fig.6.9

7. Summary

In conclusion we carry out the comparison of the combinatory method with the other methods. Afterward we summarize the main results obtained in the work.

The combinatory method is in comparison with Shannon's method more general in the sense that the solutions obtained with Shannon's methods are also obtained with the combinatory method with the special operations employed therewith. Lunc's method starts with a given solution, and consists in a method of its improvement. In each stage of this procedure we get a separate solution. The combinatory method is a different type from Lunc's method: it starts "with clean paper". The construction of the scheme proceeds by steps, so that in its individual states we cannot speak of a solution but only of partial solutions. The two methods are equivalent in the sense that they enable the general structure of the solution to be obtained. The combinatory method, however, has the advantage that it is easier to survey, and it is also suitable for the machine.

The main results of the work may be summarized as follows:

First Problem: The combinatory method develops the general arrangement of the structural elements. The arrangement of the elements depends not on the algebraic

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form of the switch function but on the local characteristics of the scheme. It can be shown that the method of development of the construction of any form of scheme solves the given problem. It is usually advisable to select the sequence of operations as much as possible in such a way as to obtain a good solution. In the work the question of multiple utilization of the structural elements is also partially solved. This is accomplished, on the one hand, by using an indefinite switch function, and, on the other hand, by starting the construction of the solution with what is given, i.e., the output poles - contrary to the usual procedure.

Second Problem: The procedure described in the method is general to the extent that it is applicable to any phase of the problem of synthesis of the individual scheme as well as to every stage of the solution of the given synthesis.

The author indicates in the method the general direction to be pursued at the solution when it is desired to come as close as possible to the required form of the solution. Moreover, the method dispenses with the use of algorithm, which would necessitate in every stage of the solution a further operation, with gradual approach to the final solution. During the solution, of course, stages occur where evaluating operations are difficult. The solution is carried out by a series of trials. At each trial we construct a complete solution. The greater the number of trials is, the greater is the probability of getting a better result. The quality of the solution also depends to a considerable extent on the experience of the operator. From this viewpoint, therefore, the combinatory method is a trial or inductive method.

Because the method is sufficiently general and simple, and uses tabular forms of the switch functions, it is also suitable for the machine.

8. Acknowledgement

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Appendix

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At the suggestion of candidates Z.Korvas and K.Kristouf the author appends an example of the construction of a scheme which is not selected at random, which is more complicated than the examples in part 6 of the preceding work, and has practical employment. This is the decoder from the Powers code to the code 8, 4, -2, -1, in the normal form and in the supplement. Code 8, 4, -2, -1, which is known in the literature under the name of Rubinov's code, does not seem to A.Svoboda to be attributable to Rubinov.

The operational Table is also remarkable for the fact that it is fairly incomplete. Of 32 possible conditions, only 10 are utilized. This circumstance leaves open many further possibilities of solutions. We described the method of solution with reference to this contracted example because there would not be room to expand

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it here. The reader who has attentively read the description of the procedure and the examples in part 6 will understand the whole procedure and be able to reconstruct.

We give only the sequence in which the operations were carried out. At each of the operations the nodes on which the operation was carried out are connected, with the help of what $\sum$-branch the operation was carried out, and what new form of the function occurred.

The solution is represented in Fig.3. It was obtained in this form after the third trial.

The relay scheme is represented in Fig.4. The pair of switch elements x_i, $\bar{x}_i$ with one common node can be formed by one switch with contact.

	$z_1 z_2 z_3 z_4 z_5$	$X_1 X_2 X_3 X_4 X_5 X_6 X_7 X_8$
0	0 0 0 0 0	0 0 0 0 I I I I
1	I 0 0 0 0	0 I I I I 0 0 0
2	I 0 0 0 I	0 I I 0 I 0 0 I
3	0 I 0 0 0	0 I 0 I I 0 I 0
4	0 I 0 0 I	0 I 0 0 I 0 I I
5	0 0 I 0 0	I 0 I I 0 I 0 0
6	0 0 I 0 I	I 0 I 0 0 I 0 I
7	0 0 0 I 0	I 0 0 I 0 I I 0
8	0 0 0 I I	I 0 0 0 0 I I I
9	0 0 0 0 I	I I I I 0 0 0 0

Fig.1 - Operational Table of Decoder from Power's Code to Rubinov's Code in Normal Form and in Supplement

Remarks

1. From analysis of the scheme of Fig.4, it follows that the physical function of the decoder can give five relays to four switch contacts. This is advantageous only when such standard relays are available. It seems that in this form this decoder has not so far been solved.

2. The solution is remarkable for the fact that it is fairly advantageous but complicated, and that it enables the transformation of one standard code (Powers') to another standard code (8, 4, -2, -1).

SUMMARY

The article describes an inductive combinatorial method for the synthesis of switching circuits with one input and m output terminals which, unlike other current-

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ly known methods, does not use the methods of Boolean algebra. The method employs a simple symbolic. It is here presented as a method for computation by human operator, but is also suitable for machine, i.e., after supplementing the process of solution a suitable machine can be designed. It can be proved that by use of this method it is possible to obtain every possible structure of solution which satisfies the problem. The present method is the first which proceeds from the functions given at the output terminals to those at the input. In this it differs from the majority of methods in which the starting point is some solution determined deductively, which is then successively simplified by some procedure.

The described method is that general that it is applicable for any presentation of the above problem, and is distinguished by the fact that the same procedure is constantly repeated during the development of the solution. This fact, together with the expression of the indeterminate functions in tabular form permits of the construction of a machine for automatic synthesis.

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a)	b)	c)	d)
ω_2	X_3^1, U_0	$f_1 = x_4 + x_5$	X_3^2
ω_2	X_3^2, X_7^1	$f_2 = x_4$	X_7^2
ω_2	X_1^1, U_0	$f_3 = x_3 + x_5$	X_1^2
ω_2	X_1^2, X_3^1	$f_4 = x_3$	X_3^2
ω_2	X_3^2, X_6^1	$f_5 = x_3$	X_6^2
ω_1	X_3^2	$f_6 = \bar{x}_3$	F_1^1
ω_2	F_1^1, U_0	$f_7 = x_3$	F_1^2, X_3^3
ω_2	F_1^2, X_3^1	$f_8 = \bar{x}_4$	F_1^3, X_2^2
ω_2	X_2^2, X_5^2	$f_9 = x_4$	X_2^3
ω_1	X_6^2	$f_{10} = \bar{x}_3$	F_2^1
ω_2	F_2^1, U_0	$f_{11} = x_2$	F_2^2, X_6^3
ω_2	F_2^2, X_7^2	$f_{12} = \bar{x}_4$	F_2^3, X_7^3, X_5^4
ω_1	X_1^2	$f_{13} = \bar{x}_3$	F_3^1
ω_1	X_4^1	$f_{14} = x_1$	F_4^1
ω_2	F_3^1, F_4^1	$f_{15} = \bar{x}_2$	F_3^2, F_4^2, X_4^3
ω_2	F_1^2, F_4^2	$f_{16} = \bar{x}_5$	F_1^4, F_4^3
ω_1	X_4^2	$f_{17} = x_1$	F_5^1
ω_2	F_5^1, X_6^1	$f_{18} = \bar{x}_1$	F_5^2
ω_1	X_5^2	$f_{19} = \bar{x}_4$	F_6^1
ω_1	F_5^2	$f_{20} = \bar{x}_5$	F_7^1
ω_1	F_7^1	$f_{21} = \bar{x}_4$	F_8^1
ω_1	F_8^1	$f_{22} = x_3$	F_9^1
ω_2	F_9^1, U_0	$f_{23} = \bar{x}_2$	$F_9^2, F_8^2, F_7^2, F_5^3, X_6^3, F_2^4, X_7^4, X_4^3, F_4^4, F_3^3, X_1^3, F_1^3, X_3^4, X_2^4$
ω_1	X_8^1	$f_{24} = x_1$	F_{10}^1
ω_2	F_{10}^1, U_0	$f_{25} = x_2$	F_{10}^2, X_8^2
ω_2	F_{10}^2, F_9^2	$f_{26} = x_3$	F_{10}^3, X_8^3
ω_2	F_{10}^3, F_8^2	$f_{27} = x_4$	F_{10}^4, X_8^4
ω_2	F_{10}^4, F_7^2	$f_{28} = x_5$	F_{10}^5, X_8^5
ω_2	F_{10}^5, X_4^3	$f_{29} = \bar{x}_1$	F_{10}^6, X_4^4
ω_1	X_8^2	$f_{30} = \bar{x}_1$	F_{11}^1
ω_2	F_{11}^1, F_6^1	$f_{31} = \bar{x}_5$	F_{11}^2, F_6^2
ω_2	F_{11}^2, F_2^4	$f_{32} = \bar{x}_2$	$F_{11}^3, X_8^6, F_6^3, X_5^3$

Fig.2 - Symbols Representing the Development of the Solution

a) Kind of Operation; b) Where Operation is Carried out; c) What operation is carried out; d) New forms of functions

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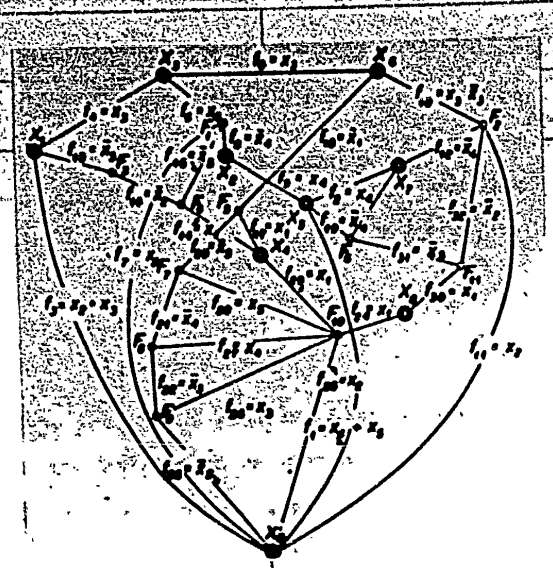

Fig.3 - Decoder from Powers' Code to Rubinov's Code in Normal Form and in Supplement

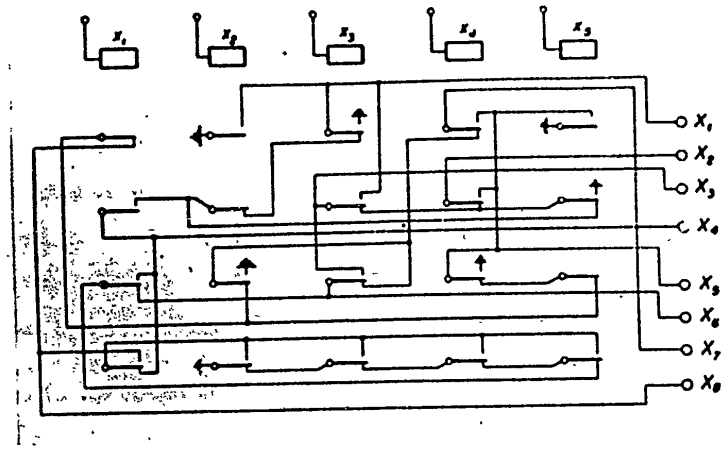

Fig.4 - Relay Scheme of Decoder of Fig.3

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THREE-PHASE HYSTERESIS CIRCUITS IN ELECTRONIC CALCULATORS*

by

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Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences

Received: 24 November, 1953

1. Introduction

1.1 Introduction. Recently, a tendency to find the most reliable solution (1.2) has appeared in the designing of the circuits of electronic calculators.

This tendency differs, for example, from the previous practice of using tripping circuits with the introduction of a system with a firm pulse governor. Most of the solutions dispense with a passive retarding member and use electronic circuits for the retardation of the individual impulses. These circuits are governed by some type of clock pulses**. The previous solutions have so far utilized regular electronic tubes. In most cases this leads to complicated, intricate circuits with a large number of electronic tubes. For the governance of these circuits, several types of clock pulses are necessary whose formation is difficult.

By the introduction of hysteresis circuits, later of hysteresis and difference electronic tubes as well as of three-phase clock pulses, the circuits have been greatly simplified. The employment of three-phase hysteresis circuits promises a high operating reliability. The circuits can work reliably at any frequency of the clock pulses (the upper limit of the employed frequency is determined only by the

* Presented to the Second Regular Whole-State Conference of the Laboratory of Mathematical Machines in December 1953

** The concept pulse is defined here as any sequence of impulses repeating periodically.

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action of the parasitic capacity). The independence of the lower limit of the frequency is due to the fact that the circuits do not contain connected condensers. The hysteresis circuit of the electronic tube has only two resistances.

1.2 Example of Previous Technique. As the example of the previous technique the electronic retardation line from Bibl.1 is taken, which illustrates very well the effort to obtain reliability at the expense of increasing the number of electronic tubes (Fig.1).

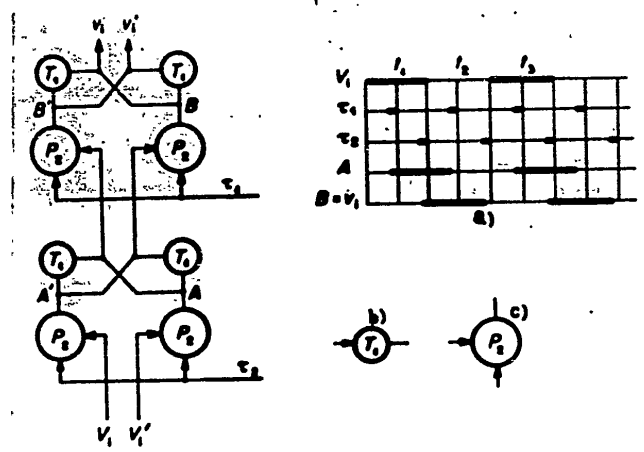

Fig.1 - Electronic Circuit for Retardation of Impulses

a) Impulse diagram; b) Triode; c) Pentode in switch connection

The circuit for retarding the impulses in time of the units of the machine is composed of two tripping circuits, each of which has two switches. Of the switches belonging to one tripping circuit, the one is always closed and the other always open. By this it is clearly determined whether the entering phase of the impulse τ will trip the circuit to the one or the other position. At a change in the conductivity the switch closest to the impulse τ automatically returns the tripping circuit to the original position. By them the output impulse is precisely derived

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from the phase pulse, and, because we have available both of its polarities (output of the tripping circuit), it can serve for dominating further similar circuits (governance of switches).

The activity of the whole retardation circuit can be best understood from the time diagram of the impulses represented in Fig.1.

The circuit has in all four triodes and four pentodes. By a similar method, the circuit containing 13 triodes and 12 pentodes is solved by algebraic addition (addition and subtraction). Moreover, this circuit may be regarded as a great improvement.

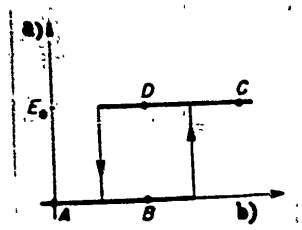

Fig.2 - Idealized Hysteresis Characteristic

a) E_{output}; b) E_{input}

Fig.3 - Impulse Diagram for Employment or Hysteresis Four-Pole

a) E_{output}

2. Utilization of Hysteresis in Electronic Circuits

2.1 Hysteresis Circuit. We have a four-pole, whose characteristic E_{output}/E_{input} exhibits hysteresis, as represented in Fig.2. The two transitions of the characteristic are unconnected.

Let us arrange this four-pole in such a way that at its input, the sum of the two voltages e_1 and e_2 is added (for example, by addition of the resistances).

Then let such a four-pole be used as follows:

In the resting position such a circuit has zero input voltage. This state corresponds to point A in the characteristic of Fig.2. When we apply either the one

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or the other input impulse we get to the highest characteristic at point B and back; the output voltage is unchanged. If at any moment both impulses are in the input simultaneously, we get via the unconnected part of the characteristic to point C. This means the output voltage changes in one leap from 0 to E_o. This voltage remains unchanged even if one of the input voltages falls to zero. This state corresponds to the characteristic of point D. It is only when the second input voltage also disappears that the output voltage again falls back in one leap to zero. This event corresponds to the characteristic of the transition from point D to point A.

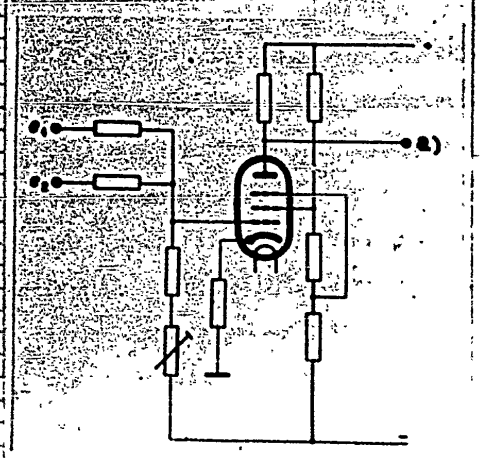

Fig.4 - Hysteresis Circuit with Pentode

a) e_{output}

For the employment of this circuit, we carry out the input voltage in the form of overlapping impulses as represented in Fig.3. Here an output impulse occurs only if there occur at the input both such timed input impulses and in temporal agreement with the last of them.

The output impulse can be directly employed as one of the input impulses of another circuit of the same type.

The existence of an output impulse is given by the simultaneous existence of both input impulses. The circuit can therefore be employed for the formation of the Boolian product of variables suitably depicted by the considered impulses. The following can therefore be written (see Bibl.3)

$$E_{output} = E_1 \cdot E_2.$$

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where E is the value of the statement of the existence of an impulse at the individual terminal of the circuit. Because of the circumstance that the output impulse endures longer than either of the input impulses, this circuit has an advantageous character for further employment.

A four-pole with a hysteresis characteristic can be obtained, for example, with the help of two-pole characteristic I/E having a negative resistance in the considered range. The existing electronic circuits which have a hysteresis characteristic are suitable for this employment. This is the case, for example, with the known Schmitt circuit with two triodes (Bibl.4). A similar circuit can be formed with magnetic amplifiers or transistors. It can also be realized with one pentode (Fig.4). The idea followed at the designing of the circuit is approximately as follows: in the second and third grids of the pentode, a circuit is formed which has two stable positions and whose voltage is tripped at the first grid. The cathode resistance increases the hysteresis of the circuit (at which the application of voltage to the grid circuit depends on the state of the tripping circuit). Advantages of this type of circuit are:

1. Employment of one electronic tube. Also satisfactory here are normal high-frequency pentodes.
2. Enable direct connection between individual circuits. The circuits are thus firmly held in the given position.
3. Because of the same direction of the connections in the circuit, it is unusually stable. For example, at a change in the unidirectionally-connected voltage the influence of the voltage change on the individual electrodes is nearly compensated. The circuit is insensitive to such change until about ± 20%.
4. The input and output are separated from the tripping circuit.

A disadvantage of the circuit is that the temporal constant of the circuit, given mainly by the magnitude of the resistance in second graduations, limits the

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maximally employed frequency.

2.2 Hysteresis Electronic Tube. Consider the switching electronic tube schematically represented in Fig.5. It is composed of an electronic valve, two deviating plates and two anodes. The electronic valve* forms an electronic ray, with whose help the two plates can deviate to the one or the other anode. The arrangement of the electrodes in the electronic tube can be such that the passage of the electronic ray from the one anode to the other occurs in a leap and has a hysteresis character. (This arrangement is not shown in the figure.) Such a switching electronic tube is therefore called a hysteresis electronic tube.

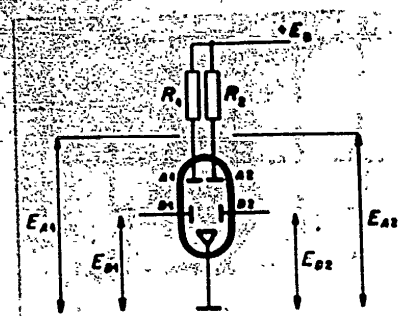

Fig.5 - Hysteresis Electronic Tube

The current characteristic of one of the anodes of the hysteresis electronic tube is represented in Fig.6. The current characteristic of the other anode is the exact mirror image, because one and the same ray falls in succession on the two anodes.

At rest the electronic ray reposes on the first anode (A1). The voltage of the first plate $E_{D1} = E_B$, the voltage of the second plate $E_{D2} = E_B - E_0$, so that $E_{D2} - E_{D1} = -E_0$ is valid. This state corresponds to point A of the characteristic of Fig.6. E_0 is the voltage of the impulse applied to the plates. We select it ten times greater than the voltage difference of the plates necessary for tripping the electronic ray from the one anode to the other.

When the voltage E_{D1} falls to $E_B - E_0$ we have $E_{D2} - E_{D1} = 0$, and the state

* The individual electrodes of the electronic valves are left out as unessential to the explanation. The system of electrodes of the three electronic valves is denoted by the triangle.

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corresponds to point B of the characteristic. The electronic ray remains on the left anode, and the output voltages $E_{A2} = E_B$ and $E_{A1} = E_B - I_A R$ remain unchanged at this. If now we increase the voltage E_{D2} to E_B, the electronic ray goes by a leap to A_2. The state corresponds to point C of the characteristic. By this the voltage on the anodes is changed. If the voltage E_{D1} again rises to E_B, the electronic ray remains on the right anode (state corresponding to point D of the characteristic). When E_{D2} falls to the original value the electronic ray again returns by a leap to A1.

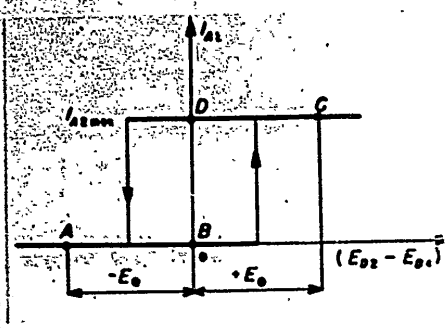

Fig.6 - Current Characteristic of Anode A2 of Hysteresis Electronic Tube

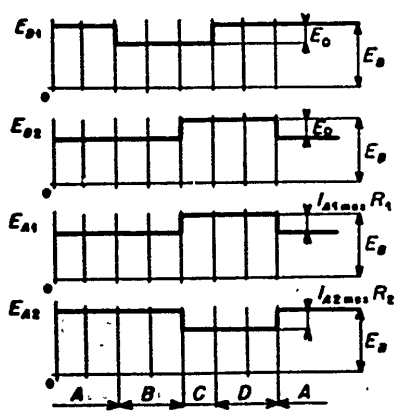

Fig.7 - Temporal Course of Voltage on Electrodes of Hysteresis Electronic Tube

Figure 7 represents the temporal diagram of the individual impulse electrodes of the hysteresis electronic tube. The individual intervals denoted A, B, C, D correspond to the individual points of the characteristic of Fig.6.

It night seem disadvantageous to employ two different courses of the voltage on the deviating plates for dominating the electronic ray. It should, however, be noted that the same course of the voltage which is employed for denominating the left plate is also that of the right anode and conversely.

If, then we select $I_A R = E_0$ (for the assumption that $R_1 = R_2 = R$ and $I_{A1max} = I_{A2max} = I_A$), we can use the output voltage directly as the input vol-

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tage of another hysteresis electronic tube. If, then, we select in principle the resting position of the electronic ray on the left (A1), then at the connection it is sufficient for the left anode always to be connected with the right plate and conversely.

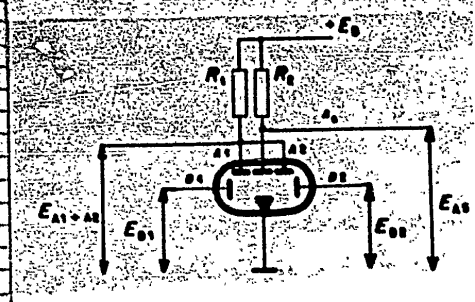

Fig.8 - Difference Electronic Tube

The electronic tube of this type can be employed similarly to the hysteresis circuit for the formation of the Boolian product.

$$E_{output} = E_1 E_2$$

Contrary to the hysteresis circuit, resistance addition is unnecessary because the electronic tube has two independent insulated inputs. This eliminates the danger of oversounds. The whole circuit of the electronic tube is composed of only two resistances.

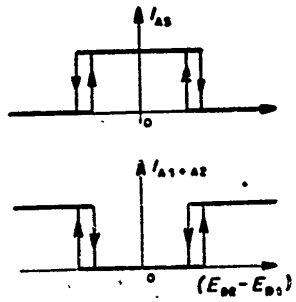

Fig.9 - Current Characteristic of Difference Electronic Tube

E_2	E_1	E_0
0	0	0
0	1	1
1	0	1
1	1	0

Fig.10 - Table Characterizing the Action of the Difference Electronic Tube

2.3 Difference Electronic Tube. For electronic circuits of this kind there

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also seems suitable another type of electronic tube, which is called the difference electronic tube.

The difference electronic tube consists of an electronic valve, two deviating plates and three anodes. The right and left anodes are connected together. The difference electronic tube is schematically represented in Fig.8.

At rest the electronic rays remain on the middle anode. The deviating plates have the same voltage.

At the arrival of only one impulse on either of the plates, the ray goes by a leap to the right or the left anode, where it remains for the time of its duration. After the end of this impulse, it again returns by a leap to the middle anode. If, however, the same impulse arrives on both plates simultaneously, its action is disturbed, and the ray remains on the middle anode. The characteristic of this electronic tube is represented in Fig.9.

On the middle anode therefore, an impulse occurs when an impulse arrives on only one of the plates. On the connected ends of the anodes a temporally-corresponding impulse of the opposite polarity occurs. This means that we have available two types of impulses as with the hysteresis electronic tube.

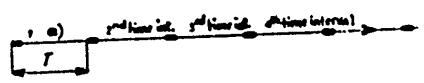

Fig.11 - Clock Pulse

a) 1st time interval

When we write the action of this electronic tube in the form of the Table of Fig.10, we see that the difference electronic tube can (similarly to the hysteresis circuit) be employed for the Boolian function which is called nonequivalence, and we write

$$E_{output} = (E_1 + E_2)$$

For the domination of the difference electronic tube, we always employ only

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simultaneous impulses and of the same type (the same polarity).

At the simultaneous employment of difference and hysteresis electronic tubes, it is advantageous to select for them the same input and output voltages. In this way the two electronic tubes can be directly connected.

3. Three-Phase Clock Pulses

3.1 Definition. The automatic calculator has heretofore employed only the fundamental type of clock pulses, from which the remaining necessary impulses have been derived (Fig.11). A clock pulse is defined here as a pulse with the fundamental

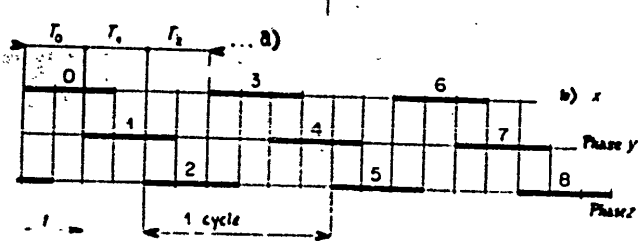

Fig.12 - Three-Phase Clock Pulses

a) Time intervals; b) Phase x;

frequency which governs all of the events of the calculator.

In contrast, the three-phase hysteresis circuit employs three kinds of clock pulses of the same frequency and alternation (1:1) but with the phases mutually displaced 120° (Fig.12). It has been found that with these pulses together with the hysteresis circuit, the calculating circuit can be developed in a very flexible manner.

The individual pulses are, in accordance with the usual practice of electrotechnology, denoted phases x, y, z. All of the clock impulses are numbered from the selected moment in the sequence in which they issue from the generator of clock

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pulses regardless of their phase (see Fig.12). For the first number we select 0, which we denote the selected impulse of phase x. If the sequence of the impulses of the phases is x, y, z, then it is valid that in phase x all are 3n-th impulses, in phase y all are 3n + the first, and in phase z 3n + the second, where n is a whole positive number.

The time interval between the first two neighboring impulses is called (simply) the time interval, and we number it in agreement with the number of the pulse which begins in the same moment as the time interval. The time interval between the first two neighboring impulses of the same place is called the cycle.

Fig.13 - Symbol of Hysteresis Electronic Tube

The clock impulses are denoted below directly by the symbols of the phases.

3.2 Symbolism. The circuit is designed in such a way that in the same node an impulse of one and the same node always occurs.

By the Boolian variable a, we denote the presence (a = 1) or the absence (a = 0) of an impulse in the node a. Actually, the fact that we employ for the denotation of the variable the same symbol as for the denotation of the corresponding node is advantageous, because in this way the correspondence between the node of the scheme and the corresponding variable of the equation is directly determined.

Fig.14 - Symbol of Difference Electronic Tube

The variable a is supplemented with the index t, which denotes the number of the clock impulse, and with the index f at the left and raised, which denotes the phase, thus: ${}^{f}a_{t}$

Fig.15 - Circuit for Retardation of Impulses by 1 Time Interval

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If the scheme has a large number of anodes, it is advantageous to number these anodes. Then

"125" (read impulse 15 in node 125 of phase x)

symbolises the impulse simultaneous with the impulse 15 (which is in phase x) of the clock pulse in the node 125. The phase index f can be derived from the index t, and is added only when it is necessary for the good legibility of the scheme.

With the help of this symbolism we describe the action of the hysteresis electronic tube (schematically represented in Fig.13).

We denote one of the deviating plates a, the other b, the output node c.

Then the following is valid

$$c_{n+1} = a_n b_{n+1} = (ab)_{n+1}$$

or

$$c_{n+1} = a_{n+1} b_n = (ab)_{n+1}.$$

The action of the difference electronic tube (schematically represented in Fig.14) described by this symbolism is as follows: if a and b are the individual plates and c is the output node, then the following is valid

$$c_n = (a_n \not\equiv b_n) = (a \not\equiv b)_n.$$

3.3 Simple Example of Employment of Three-Phase Hysteresis Circuit. Retardation of impulse by one time interval. The retardation of the impulses of the hysteresis electronic tube is carried out by the introduction of a suitable clock pulse at one of its inputs. Figure 15 shows an example of the retardation of the impulse 3s (phase x) with the help of the clock pulse y (next phase). For the resultant impulse in the next time interval and in the next phase, the following is valid:

$$^{y}b_{3n+1} = {}^{x}a_{3n}y.$$

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Retardation of One Cycle. The retardation by one cycle (i.e., by three time intervals) is carried out with a cascade of three circuits retarding by one time interval (Fig.16). The detailed scheme of the connection of the hysteresis electronic tube in the circuit with retardation by one cycle is shown in Fig.17.

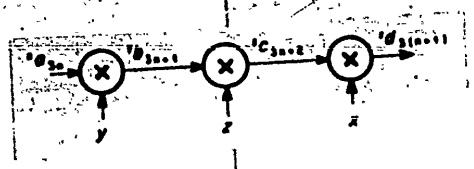

Fig.16 - Circuit for Retardation of Impulses by One Cycle

Retardation Line. By the employment of n hysteresis electronic tubes, a line with retardation by n time intervals can be formed. By the introduction of backward

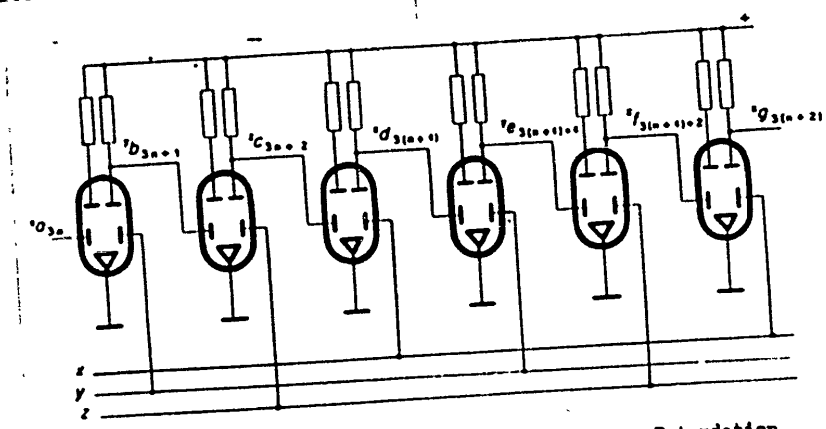

Fig.17 - Scheme of Connection of Three-Phase Retardation Line

links (for the case where the line retards by 3k) we form a serial memory for the word with k binary digits. The retardation line is represented in the scheme of Fig.18, where the symbol Δ denotes the retardation line, the index on the right below the number of time intervals n by which the impulses are retarded.

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Circuits for Particular Employments of Retardation Lines. The three-phase retardation line has the advantageous characteristic that the working arent can be blocked at any time, for example, with the circuit represented in Fig.19. At this a retardation occurs which is independent of the length of the line, which can be managed by the machine.

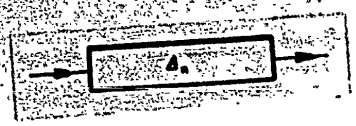

Fig.18 – Symbol of Three-Phase Retardation Line Retarding by n Time Intervals

Such a circuit can be advantageously employed for transforming serially- to parallelly-depicted numbers, and conversely. This transformation can be carried out in any cycle which the machine can manage.

This circuit can also be employed for conversion of slow to rapid data, and conversely (replacement of output data in the ultrasound memory, output from the memory, and the like). In the blocked line, parallelly-depicted numbers can be put

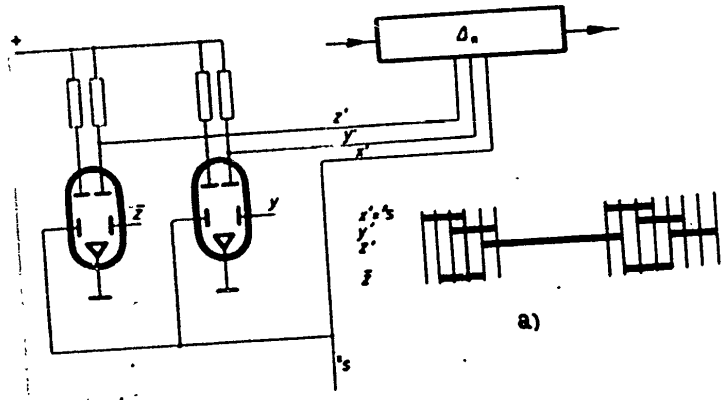

Fig.19 – Circuit for Blockage of Traces of Impulses Arriving in the Retardation Line

a) $\bar{z}$ is the supplementary pulse of the clock pulse z

in, which can be taken out at the right moment at full speed in the form of serially-

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depicted numbers.

Figure 19 shows the dominating circuit of this retardation line. Until the arrival of the moving impulses x_s at the input s of this circuit, the line is in normal operation. When the impulse x_s is blocked it is retained in the electronic-tube phase z (as shown by the time-impulse diagram of Fig.19, pulse z') until the arrival of the next impulse x_s. At the emission of n, therefore, this impulse acts on the output of the line with a retardation of n cycles. The block retardation line may also be regarded as a parallel memory, into which n impulses x_s of numbers displaced by n places can be introduced.

Formation of Supplementary Pulse. The difference electronic tube can also be advantageously employed for the formation of supplements, i.e., by introducing at one of its inputs a clock pulse of the same phase as the impulse at the other input (Fig.20). We have here

$$\bar{a}_{3n} = ({}^{s}a_{3n} \not\equiv x),$$

so that $x_{\bar{a}3n} = x_{b3n}$.

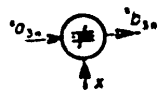

Fig.20 - Circuit for Formation of Supplements

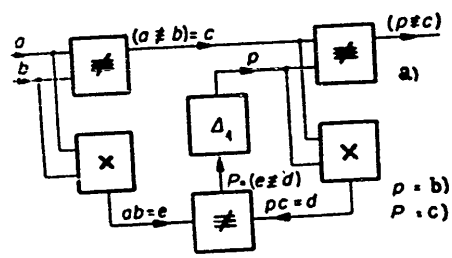

Fig.21 - Logical Scheme of Serial Binary Addition

a) Sum; b) Old transfer; c) New transfer

Serial-Binary Addition. Figure 21 shows the logical scheme of the circuit of binary serial addition. Figure 22 represents the scheme of three-phase binary serial

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addition for the logical scheme of Fig.21 employing hysteresis and difference electronic tubes. In large schemes it is usually advantageous to arrange the electronic tubes through which the input pulses pass in the same time interval in such a way that they are always above each other. This is also the case with the scheme of this addition. From the scheme, for example, it can be clearly seen that the transferred pulse j_7 encounters not the impulse d_4 but the impulse which arrives at the node d retarded by a cycle, i.e., in the time interval 7.

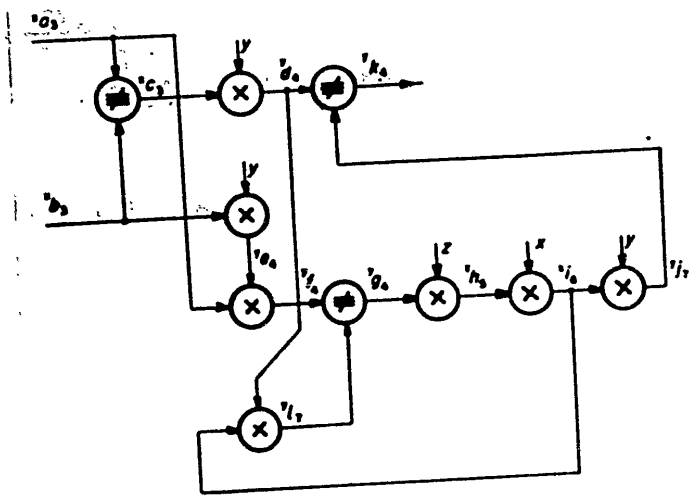

Fig.22 - Scheme of Three-Phase Serial Binary Addition

It should be noted that in the circuit there are fully sufficient ten electronic tubes of the two mentioned types.

4. Employment of Proposed Three-Phase Hysteresis Circuit for Synthesis of Pulses of Complex Impulse Sequences

4.1 Example. The three-phase system also enables the synthesis of circuits forming complex sequences of impulses. We take a fairly simple example of a circuit forming impulse sequence whose formation by the usual means leads to a considerably more complicated circuit.

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Figure 23 represents a retardation line retarding by 3 k time intervals. The output A is connected with the input of the line. The branch line B is connected with any node inside the line.

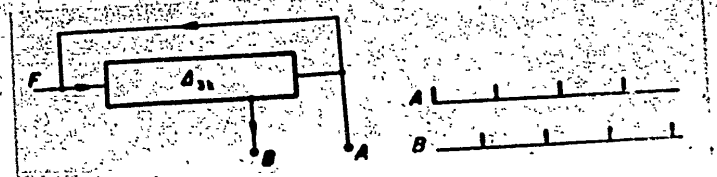

Fig.23 - Circuit Employed for Synthesis of Pulses of Complex Impulse Sequences

If we put the starting impulse f_F in this circuit, an impulse which is repeated in every k^{th} cycle is formed in the beginning at the output A (see the impulse diagram of Fig.23). At this the impulse at the output B is again repeated after every

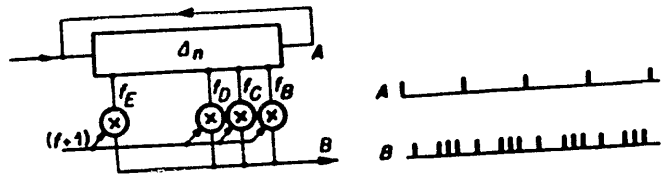

Fig.24 - Example of Synthesis of Pulses of Complex Sequences

k^{th} cycle but in relation to the impulse f_A displaced by the total number of time intervals. It is clear that with the help of this circuit, nodes of various phases in the retardation line can be selected, forming, for example, also pulses whose impulses have a length of several time intervals.

Figure 25 represents the connection of two circuits of Fig.23. The retardation line of the left-hand circuit retards by n cycles, that of the right-hand one, by m cycles, at which n and m are noncooperating numbers. When starting impulses are put

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into these connected retardation lines, coincidence occurs, in the points A and B in every mn^{th} cycle.

By the selection of a suitable pair of outputs (the one on the left and the other on the right of the retardation line, we can obtain coincidence of two impulses

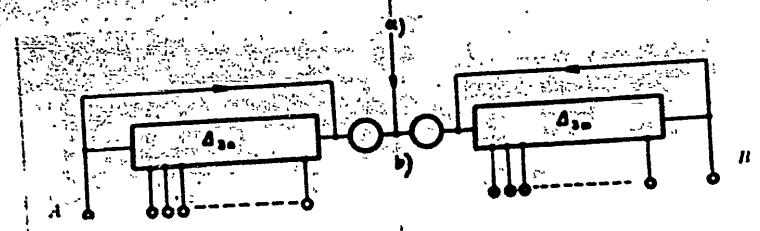

Fig.25 - Circuit Employed for Synthesis of Long Pulses of Complex Impulse Sequences

a) Starting impulse; b) Graduated separation

displaced by any number of cycles relative to the coincidence in the points A and B. Coincidence of the pulses at any outputs selected in this way is again repeated

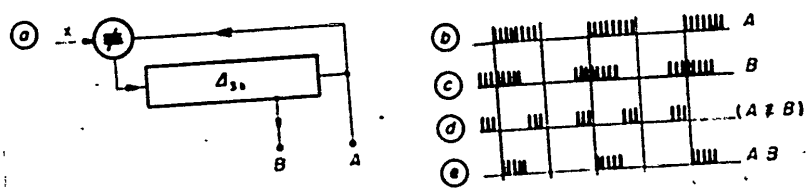

Fig.26 - Circuit Employed for Synthesis of Pulses of Complex Impulse Sequences

after n · m pulses.

Figure 26 represents another connection of the retardation lines and different electronic tubes. The left input of the difference electronic tube is connected with the source of clock pulses x and the right input with the output of the retard-

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ation line. The input of the retardation line is connected with the output of the difference electronic tube.

At the output A knots of clock pulses occur periodically (Fig.26b), at the output B pulses of the same phase with displacement of the knots occur (Fig.26c).

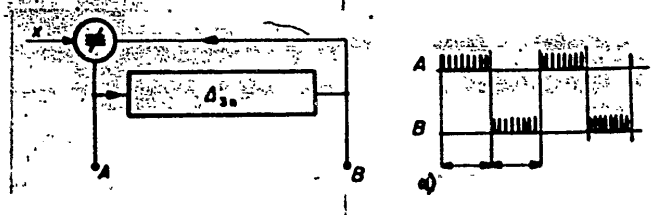

Fig.27 - Circuit for Classification of Even and Odd n^{th} Clock Pulses

a) n impulses

We add some further simple circuits with which pulses of various complex sequences can be obtained. Figure 26d shows the pulses occurring when the outputs A and B are connected with a difference and a hysteresis electronic tube.

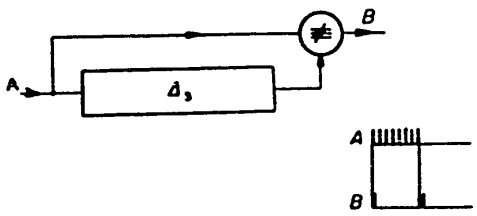

Fig.28 - Circuit for Formation of Identified Impulses

Figure 27 represents a circuit for classifying even and odd n^{th} pulses.

Figure 28 represents a circuit which at the beginning and the end of a series of impulses puts out identified impulses.

5. Discussion

Three-phase hysteresis circuits may be expected to be highly-reliable circuits. The impulses dominating the electronic tubes are not only signals of changes in state but they also maintain the electronic tubes in the working state. The events

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in the machine are firmly governed. All of the impulses, with the exception of some control impulses, are either three-phase clock impulses or are directly derived from them. The output impulses of any electronic tube are wholly new; with both the hysteresis and the difference electronic tube the characteristics of the ascending and descending edges are unconnected with each other. The three-phase hysteresis circuit works at any frequency (limited upwardly) of clock pulses, which facilitates synchronization with other parts of the calculator, for example, with ultrasound memories and the like.

The described electronic tubes, dominated by three-phase clock pulses, represent two types of standard, universally-exployable structural units of the circuits. At this, the synthesis of governing and calculating circuits is considerably simplified. The circuits employing the electronic tubes are very simple, being composed of only two resistances.

As we have shown in several cases, the employment of the three-phase hysteresis circuit leads to the simplification of some fundamental governing and calculating circuits. The conversion of slow to fast data and conversely, for example, the transformation of serial - to parallel - depicted numbers and conversely, facilitates the designing especially of the input and output circuits of calculators.

In the above descriptions of three-phase hysteresis circuits, we also have seen the justification of the employment of two new types of electronic tubes. Stability and reliability are such valuable characteristics of such circuits of electronic calculators that the adoption of the new system would be justified even if there were no further advantages.

In view of the fact that the electronic tubes are actually fundamental members of such circuits of electronic computers (not to mention their possible employment in multichannel pulse communication, in synchronized television, and other fields of the pulse art), they can be produced in fairly large series. In this way the greater reliability of the computer with such a circuit will match its excellent

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availability.

In the described three-phase hysteresis circuits we see a way for the construction of more reliable and more efficient electronic calculators.

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SUMMARY

The article describes a new concept in circuits for electronic digital computers, based on the use of so-called hysteresis circuits and three-phase clock pulses.

The use of two new types of electronic switching tubes in circuits controlled by three-phase clock pulses leads to the simplification of certain computing and control circuits, as is illustrated by several examples.

Below a certain limiting frequency, the three-phase hysteresis networks work at any frequency (down to zero) of the clock pulses. This enables simple data-speed conversion and the parallel-to-series transformation (and vice-versa), etc. The circuits permit the simple synthesis of complicated pulse trains and pulse-delay by electronic means (the circuits do not use passive delay elements at all).

The hysteresis circuit is held in both of its states by the input signal (in opposite to ordinary flip-flops), and it is therefore expected to be highly stable.

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ELECTROMAGNETIC RELAY WITH SUPPRESSED INDUCTIVE CONNECTION BETWEEN WINDINGS

by

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Received: 5 January, 1954

Introduction. A fundamental structural element of relay machines for the processing of information is the electromagnetic relay. In this application the relay must satisfy high demands with respect to reliability and speed. The more rapid the relay is, the more information the machine can process; the more reliable it is, the fewer errors the machine will make at this processing.

The subject of this article is an electromagnetic relay with suppressed inductive connection between the windings, which, according to experiments carried out, is more advantageous than the normal relay for machines for processing information. Its superiority consists in that it entirely eliminates the error due to the inductive connection between the windings, and thereby enables full utilization of its working speed.

In the first part, the method of feeding and connecting the relay in the relay network of the machine for processing information as worked out by Antonin Svoboda is described. The second part deals with the errors in the action of the machine due to the influence of the inductive connection between the windings of the same relay and the method of their elimination. In the third part, the relay with suppressed connection is described, and, finally, the fourth part contains the results of the laboratory experiments carried out.

1. Connection of Relay in Machine for Processing Information. There are many

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possibilities for the connection of the relay circuit. The present article is concerned with a connection which uses a relay with two windings. The relay is fed with a system of electrical pulses in such a way that the switching of its contact occurs without sparking when no current is passing through it. This decreases very considerably the necessary contact and increases the reliability of the relay circuit connected in this way.

The important parts of the relay are the working winding, the holding winding, and the row of contacts. Figure 1 represents the scheme of a relay with five switching contacts. When the working winding receives electrical impulses the relay attracts the armature and switches the contact. At this the holding winding is

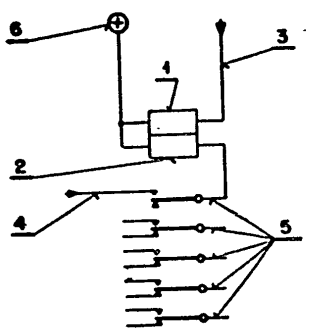

Fig.1 - Scheme of Relay

1 - Working winding; 2 - Holding winding; 3 - Inlead of working pulses; 4 - Inlead of holding pulses; 5 - Contact; 6 - Permanent connection of positive pole of source

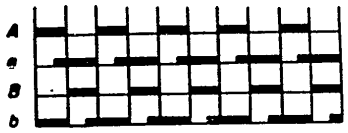

Fig.2 - Time Diagram of Pulses

connected with the inlead of the holding pulses. After the arrival of the holding

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impulse, the relay remains in the working position for the duration of the holding impulse.

The feeding of the relay circuit occurs with a system of unidirectional electrical pulses, whose time diagram is represented in Fig.2. The basis of the pulse system consists of the forms of pulses denoted A and B. Each of them is formed by a regular sequence of impulses of the same kind and of the same length as the gaps between them. The pulses A and B are displaced in time in such a way that the impulses of pulse A just fill the gaps of the pulse B and conversely. If we know the time which the relay requires for attracting or falling off, it is sufficient to select the length of the individual impulses of the pulses A and B only a little greater than the greater of the two times. The pulses A and B are supplemented by the holding pulses a and b. The pulse a is formed by a regular sequence of impulses, which supplement the impulses of the pulse A. The impulses of the pulse a, begin in the last third of the impulses of the pulse A and endure until the beginning of the next impulse of the pulse A. The pulse b supplements similarly the pulse B. The pulses A and B are conducted to the working winding of the relay, the pulses a and b are conducted to the holding winding of the relay.

Each relay is therefore in principle composed in such a way that via the contact the relay whose working winding is fed with pulse A conducts and the pulse, and, conversely, via the contact the relay whose working winding is fed with the B conducts the pulse A. The holding winding of the relay fed with the pulse A is via a special contact connected with the pulse a. Similarly, the holding winding of the relay fed with the pulse B is via a special contact connected with the pulse b. The pulses A, B, a, b, are produced by the generator of pulses. The generator of pulses is the only place where the current is connected or disconnected. The contacts of all of the relays are always switched in a moment when no current is passing through them.

Figure 3 represents the connection of a relay network fed according to the

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described principle. In this figure the current source, the generators of the pulse A, a, B, b and the relays are represented, divided in several groups according to the pulses with which they are fed. The rectangles denoted 2 and 4 in the figure

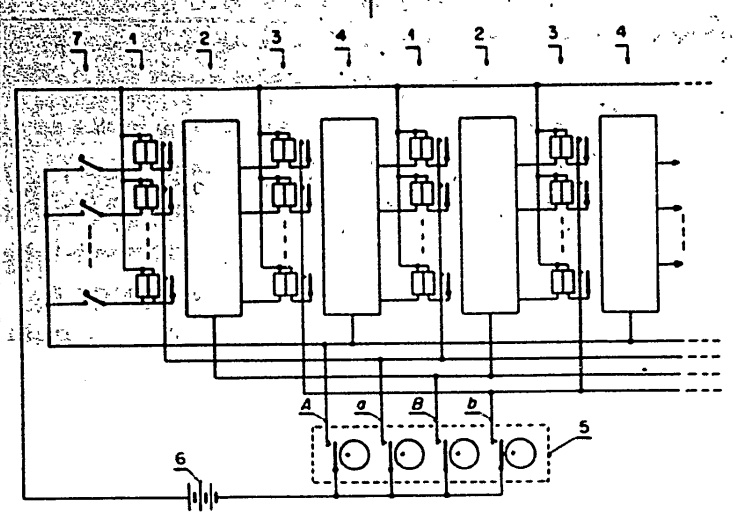

Fig.3 - Block Scheme of Relay Network

1 - Relays attracted by pulse A; 2 - Contacts of relays attracted by pulse A; 3 - Relays attracted by pulse B; 4 - Contacts of relays attracted by pulse B; 5 - Generator of pulses; 6 - Source; 7 - Input arrangement

take the place of the detailed depiction of the connections of the contacts of the relays. These connections will differ from case to case, and have nothing to do with the feeding of the relay network. Each relay group belongs in the figure to one such rectangle. Its input is connected with the generator of pulses, its outputs are connected with the working windings of the relays of the next group. After starting the generators of pulses the impulses of the pulse A of that relay of the first group (on the left) start, which is through the input arrangement 7 connected

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with the pulse A. The started relay holds the next impulse of the pulse a and forms by its contact the path for the pulse B to the working winding of some relay of the second group (from the left). Over the prepared path the impulses of the pulse B go to the selected relay of the second group. After the end of these impulses, the the impulses of the pulse a also end, whose relays of the first group first hold and then drop them. The started relay of the second group then holds the corresponding of the pulse b and forms with its contact the path for the pulse A to some relay of the third group, etc. Thus the information put into the relays of the first group in the beginning is processed by the relay network in the manner indicated in the detailed connections of the contacts of the relays of the individual groups.

2. Errors Due to Inductive Connection between Windings of Same Relay. An indispensable but sufficient condition for the proper functioning of a relay network of the described type is that all of the relays fall off in the time given by the gaps between the impulses of the holding pulses a, b, and are only attracted impulses from the generator of pulses arriving in their working windings. If the relay network is composed of a large number of relays in complicated connection, it sometimes happens that during the action of the network some relay does not fall off in time, or conversely, attracts at a time when it is not connected with the generator of pulses at all, so that it should remain at rest. Both of these phenomena occur as the result of certain defects of the relays of the machine. A defect of this kind is due to the inductive connection between the windings of the same

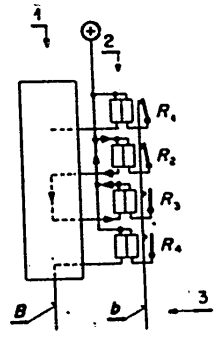

Fig.4 - Occurrence of Closed Circuit in Relay Network

1 - Contacts of relays attracted by pulse A; 2 - Relays attracted by pulse B (R_1,R_2,R_3,R_4), 3 - Arrival of pulses

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relay. A relay with two windings behaves like a transformer, at which any change in the current in the one winding induces voltage in the other winding. If at the moment the current is closed in the second winding, current flows through it, which brings about either a delay in the falling-off of some relay which should fall off just then or an unwanted attraction of some other relay. An example of such a critical situation is represented in Fig.4. Here are shown four relays of one group connected by the contact network of the relays of the preceding group with the pulse B. Since what is concerned here is a network of the already-described type (Fig.3), it is clear that the relays of the preceding group not shown in Fig.4 are connected in a similar way with the pulse A. We are interested in learning what happens at the moment when the holding of the impulses of the pulse b ends. The relays R_1 and R_2 have just been attracted by the impulses of the pulses B and are held by the holding pulse b. The contact of the relays of the preceding group ceases just during the impulses of the pulse A, so that the connection indicated by the dotted lines in the rectangle 1 of Fig.4 forms. At the moment when the impulses of the pulse b ends and the impulses of the pulse B begins, a harmful connection between the windings occurs. The relay R_4 attracts normally, and the relay R_1 falls off likewise normally. However, the relay R_2 has its working winding connected with the close circuit via the working winding of the relay R_3 and both are receiving positive voltage. The voltage induced in the working winding of the relay R_2 at the interruption of the current at the end of the impulses of the pulse b suppresses this circuit of the unwanted current in the manner indicated by the arrows in Fig.4. This current, on the one hand, delays the falling-off of the relay R_2, and, on the other hand, tries to attract the relay R_3, which, however, remains at rest.

The situation just described may occur at many places of the relay network, and especially when the network contains a large number of relays in complicated connection. Here, therefore, during the action of the relay network parallel con-

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nection of a large number of relays may occur. The latter varies, depending on whether at the beginning of the closed circuit the majority of the relays are in the working or in the resting position. In the circuit of the working winding of the

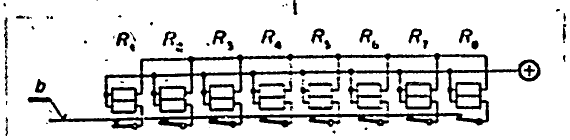

Fig.5 - Connection of Majority of Attracted Relays

fallen-off relay R_1, however, a small resistance is present (the windings of all of the relays R_2-R_8 are connected in parallel), by which its falling-off is delayed in such a way that the relay R_1 is unable to fall off in the gap between the impulses of the pulse b, so that it holds during the whole interval of the next impulse. In both cases the machine makes errors.

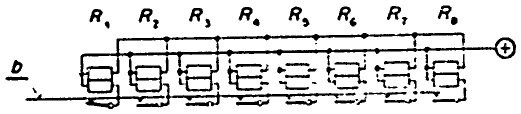

Fig.6 - Connection of Majority of Fallen-off Relays

In all, four ways to eliminate the errors due to induced current are known: 1. lower the speed of the generator of pulses and therewith also the speed of the machine; 2. include resistances limiting the magnitude of the induced current; 3. designing a better scheme; and, finally 4. using relays with suppressed inductive connection between the windings.

By lowering the speed of the generator of impulses, the duration of the impulses and the gaps between them is lengthened. This is obtained by making the gaps between the holding impulses longer than the falling-off time of the relays, whose

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windings are shortcircuited, so that errors cannot occur. In actuality, this means that the relay network works about four times more slowly than follows from the working speed of the individual relays.

By including a resistance in a series of working and holding windings, the magnitude of the induced current is limited. This can be obtained in such a way that the falling-off time, lengthened a little by this resistance, becomes less than the gap between the holding impulses. At a suitable delection of this resistance the arrangement works at full speed. A disadvantage of this expedient is the fact that the selection of the magnitude of the limiting resistance is rather critical. The whole action of such an arrangement depends strongly on the fed voltage; at a small fall the relays fail, at a rise the magnitude of the resistance is insufficient. In this case it is also necessary to lower the speed of the machine, although the slowing necessary for the reliability of the machine is not so great here as in the first case.

A suitable design of the scheme can nearly always be obtained by making it impossible for closed circuit for induced current to occur. This, however, is a very difficult condition for the designing of the relay network, and especially with respect to its main functions. It therefore usually leads to further complication of the arrangement which is already fairly complicated, and to such an increase in the number of necessary relays, that it is impracticable in the majority of cases.

As the last solution there remains the employment of a relay with suppressed inductive connection between the windings. A change in the current in the one winding does not induce voltage in the other windings, and errors of this kind cannot occur at all. A relay especially designed for this purpose is fully described below.

3. Relay with Suppressed Inductive Connection between Windings. With the suppressed inductive connection between the working and the holding winding of the same relay, various arrangements of the magnitude circuit and the windings can be

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obtained. It consists essentially in the following:

1. In the distribution of the path of the magnetic flow excited by the current in both windings;

2. In dividing the windings of the relay into parts and such a connection of these parts that the voltage induced in the part of the one current by the change in the current in the other part is destroyed by addition.

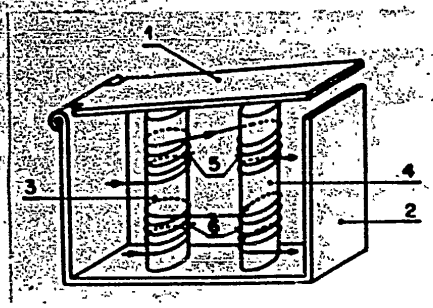

Fig.7 - Magnetic Circuit and Windings of Relay with Suppressed Connection 1 - Armature; 2 - Yoke; 3,4 - Columns; 5 - Working winding; 6 - Holding winding

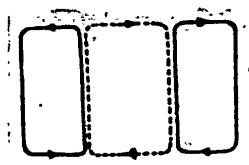

Fig.8 - Path of a Magnetic Flow in Relay with Suppressed Connection. By the dotted line the flow of the working winding is indicated, and by the solid lines the flow of the holding winding

On the basis of these principles, various constructions of the relay are possible. Some of them are described, for example, in Bibl.1. We describe below a construction which has already been formulated and successfully employed in relay circuits of the most complicated types.

The magnetic circuit and the windings of this relay are represented in Fig.7. The magnetic circuit includes an armature, a yoke and two columns. Both the working and the holding winding are divided in such a way that half of each of them is wound on the one column and half of the other column. The two halves of each of the two windings are connected with each other in such a way that the current flowing in

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the working and holding windings on the one column in the same direction flows through them on the other column in the opposite direction. The currents induced from the one winding to the other are the same but of opposite signs, so that they destroy each other.

The paths of the magnetic flow in the relay are represented in Fig.8. The flow of the working column starts at the one column, passes through the middle part of the armature, goes back to the other column, and returns from the latter to the working column. The current of the holding winding starts from both columns in the same direction, separates to the two sides of the yoke, and returns from the sides of the yoke to the two columns.

Figure 9 idealizes the courses of the voltage and current in the windings of the relay, during whose action it is assumed that the shortest-possible impulses of the types described in paragraph 1 are employed. We distinguish here three time segments. In the first time segment the impulses arrive in the working winding, current begins to flow through the latter. The current gradually increases until it reaches such a magnitude that the relay attracts the armature. The movement of the armature occurs in the moment of the drop in the current, by which the self-induction in the circuit with decreasing air gap can be explained. The second time segment begins with the arrival of the impulses in the holding winding. In this time segment the working winding

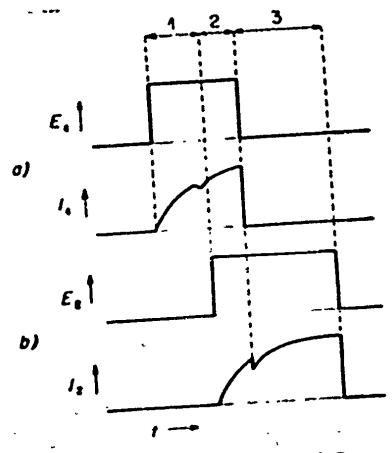

Fig.9 – Course of Voltage and Current in Windings of Relay with Suppressed Connection.

a) Course in working winding; b) Course in holding winding

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is still traversed by the current, so that it continues to attract the armature. Simultaneously, current begins to flow in the holding winding. When this current reaches a magnitude sufficient by itself to hold the armature in the attracted position, the working impulses cease, and with this the third time segment begins. During this time segment the armature of the relay remains attracted by means of the current in the holding winding. At the end of the second time segment there actually occurs simultaneously with the end of the impulses in the working winding the drop in the boosted current in the holding winding (see Fig.9b). This timing of the drop is attributable to the residual connection between the winding which was formed in the second time segment as a result of the different saturations of the two columns and the nonlinear characteristic of the iron. This phenomenon must be borne in mind at the designing of the relay, but it has no influence on the collaboration between the relays in a large relay network.

For the designing of the pulse system of a machine in which relays work with suppressed connection, the durations of the first two time segments is decisive. The first time segment must last until the armature of the relay is definitely attracted. The second time segment must last until the current which has begun to flow through the holding winding reaches the magnitude necessary for assuring the holding of the armature after the end of the working impulses. The sum of the two time segments determines the minimal length of the working impulses for assuring the proper functioning of the relays.

In comparison with the ordinary relay there is characteristic of the relay with suppressed connection a considerably longer duration of the second time segment. With the normal relay this time segment is negligibly short because its working winding is in this moment short-circuited via a small internal resistance with the source. Because the two windings have here the inductive connection in common, the current in the holding winding reaches its full value practically instantaneously*. With the relay with suppressed connection this influence (for footnote see next page)

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is, of course, absent, and the velocity of the swelling of the current in the holding winding is determined by the undiminished time constant of its circuit. The smaller working speed of the relay with suppressed connection is due to the greater share of the second time segment, but this is greatly outweighed by the impossibility of the occurrence of errors due to the inductive connection.

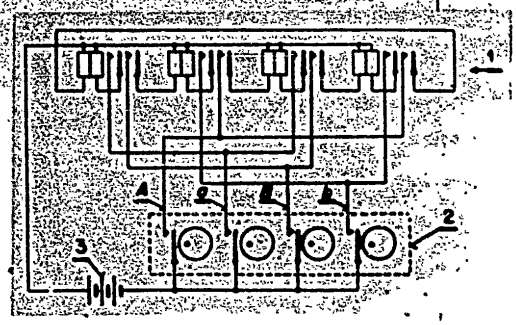

Fig.10 - Scheme of Dynamic Relay Memory

1 - Memory; 2 - Generator of pulses;

3 - Source

4. Evaluation of Relay with Suppressed Connection. In order to be able to compare the advantages and disadvantages of the method employed for eliminating the errors due to the influence of the inductive connection between the windings of the same relay, a series of measurements were carried out. Several experimental models of relays with suppressed connection according to Fig.7 were selected. The characteristics of these relays were experimentally ascertained, and compared with those of normal relays of similar construction but without suppressed connection. With relays of both kinds, a dynamic relay memory connected according to Fig.10 was formed, the functioning of which was investigated under various conditions. The relations in the actual machine were imitated, on the one hand, by shortcircuiting some of the windings of the relays, and, on the other hand, by connecting some other relays in parallel with the same pulse. The diagram of the feeding pulses was in agreement with the diagram in Fig.2, the

* As is known, the self-induction of a transformer measured at its primary terminal falls at shortcircuiting of its secondary terminal to a negligible value determined by its transformation and dispersion.

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overlapping of the working and the holding impulses was arranged with respect to the relays with suppressed connection.

The most important results of the measurements carried out are presented in the Tables of Figs.11 and 12. In these Tables, the fed voltages and the lengths of the working impulses at which the memory began to fail under various conditions of the action of the relays are given. Each line of the Tables corresponds to one measurement. The Table of Fig.11 contains the results of the measurements with normal relays, the Table of Fig.12 contains the results of the measurements with relays with suppressed connection.

From these Tables it can be seen that at 36 volts of fed voltage some of the normal reels failed at impulses of length of 6.6 ms, while the relays with suppressed connection did so already at impulses of length 7.6 ms. This disadvantage of the relays with suppressed connection was due to the length of the second time segment. When it is shortened for the windings of the normal relays, the holding impulses must be lengthened to 28 ms. By putting in experimental resistances of 270 and 500 Ω in series with the working and the holding windings respectively, the action of this relay was accelerated and shortened to 6.9 ms at 36 volts. These values depend strongly on the fed voltage, and when the latter is increased to 45 volts the speed is decreased to 13.2 ms. When a large number of further relays is connected with the same source, the voltage induced in these relays lowers the speed to 9.5-12.5 ms depending on the number of limiting resistances employed. From the Table of Fig.12, it is clear that none of the mentioned influences necessarily lowers the speed at the employment of relays with suppressed connection, which at a fed voltage of 36 volts was still 7.6 ms and at a voltage of 45 volts was 6.25 ms, which was the greatest speed reached in these experiments.

The experiments carried out show that the relay with suppressed connection satisfies the requirements specified at their employment in machines for processing information, and are actually better than the normal relays.

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a)		
b)	c)	d)
36	6,6	e)
36	28	f)
36	16	g)
36	16	h)
36	6,9	i)
45	13,2	j)
36	12,5	k)
30	9,5	l)

Fig.11 - Results of Measurements with Normal Relays

a) Measurement of normal relays; b) Voltage in volts; c) Shortest length of working impulses in millisecond; d) Remarks; e) Without shortening or resistance; f) With shortening without limiting resistance; g) With shortening and limiting resistance 270 Ω in working winding; h) With shortening and limiting resistance 500 Ω in holding winding; i) With shortening and limiting resistance in both windings; j) Same as i; k) With limiting resistance in both windings and with ten further relays connected in parallel with same source of pulses; l) With ten further relays connected in parallel with the same source of pulses, all of the relays being provided with limiting resistance

a)		
b)	c)	d)
36	7,6	e)
36	7,6	f)
36	7,6	g)
45	6,2	h)
45	6,2	i)
45	6,2	j)

Fig.12- Results of Measurements with Relays with Suppressed Connection

a) Measurement of relays with suppressed connection; b) Voltage in volts; c) Shortest length of working impulses in milliseconds; d) Remarks; e) Without shortening; f) With shortening without limiting resistance; g) With shortening without limiting resistance with ten relays in parallel; h) Without shortening; i) With shortening without limiting resistance; j) With shortening without limiting resistance, with ten relays in parallel

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SUMMARY

The article describes a new type of electromagnetic relay. The relay eliminates errors in the operation of information processing machines caused by the mutual inductance between the main and holding winding of the same relay.

The first part describes the method of energizing the relays and their connection in the relay network. The second part discusses errors in operation of the machines due to inductive coupling between the windings of the same relay, and the method of eliminating them. The third part describes a relay with suppressed coupling. The fourth part contains the results of laboratory measurements.

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STATISTICAL ANALYZER*

by

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1. Statistical Analyzer. The statistical analyzer is a machine which serves to facilitate the statistical investigation of phenomena. At the investigation of such phenomena, a rectangular field of the machine is observed in which the histogram of the frequency is composed of vertical dark strips.

The histogram is always composed of n elements of the fundamental collection. The machine changes the histogram continuously in such a way that for every k^{th} element added to the corresponding frequency one element is again subtracted from the frequency corresponding to the (k + n)th element of the fundamental collection. This machine is therefore particularly suitable for the investigation of phenomena whose characteristics depend on the order of the elements.

2. Characteristics of the Statistical Analyzer. At this description of the characteristic of the statistical analyzer we use the usual statistical terminology.

The characteristics of the phenomena are ascertained by measurement, classification and the like of the elements of the investigated collection. The investigated collection is composed of n elements of the fundamental collection, where n gives its extent. The characteristics are determined by ascertaining the frequency of the marks. The mark is ascertained by measuring some physical magnitude (for example, the diameter of a produced shaft), at which each mark corresponds to an

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interval (usually small) of the measured magnitude. With an unconnectedly-changing magnitude (for example, at the ascertainment of the number of infalls) the mark is directly the value corresponding to the concerned variable.

We have a five-place perforated tape (for example, from a telewriter). If we hold the tape vertical, each line of this tape corresponds to one element of the fundamental collection. The combination of perforations in this line represents the corresponding mark of the element. The 32 possible combinations of these perforations therefore correspond to 32 strips of the histogram in the rectangular field of the machine, whose protrusion depicts the frequency of the occurrence of the corresponding mark in the investigated collection. The order of the elements of the fundamental collection whose marks we ascertain in succession, is the same as the order of their marks on the tape.

The methods of ascertaining the marks (measurement of dimensions, measurement of time intervals, ascertainment of colors, etc), and the expression of the corresponding perforations in the perforated tape, depend on the kind of statistical units, on the investigated characteristics, and in further special requirements, which vary from case to case, and are outside the scope of the present article. We ascertain the mark with the help of some physical dimension, and assume that the measured values are perforated in the tape in the binary code.

The histogram composed of the first n elements of the fundamental collection is called the first picture. The picture formed by adding further, i.e., the (n+1)th element and subtraction of the first element of the fundamental collection is called the second picture. The kth picture of the histogram is therefore formed by adding the mark of the (k + n + 1)th element and subtraction of the mark of the (k + 1)th element of the fundamental collection.

The tape with the perforated marks of the elements enters the machine, where it is palpated and read with two sets of needles. At this, when the first set of needles reads the perforated mark of the hth element the second set reads the mark

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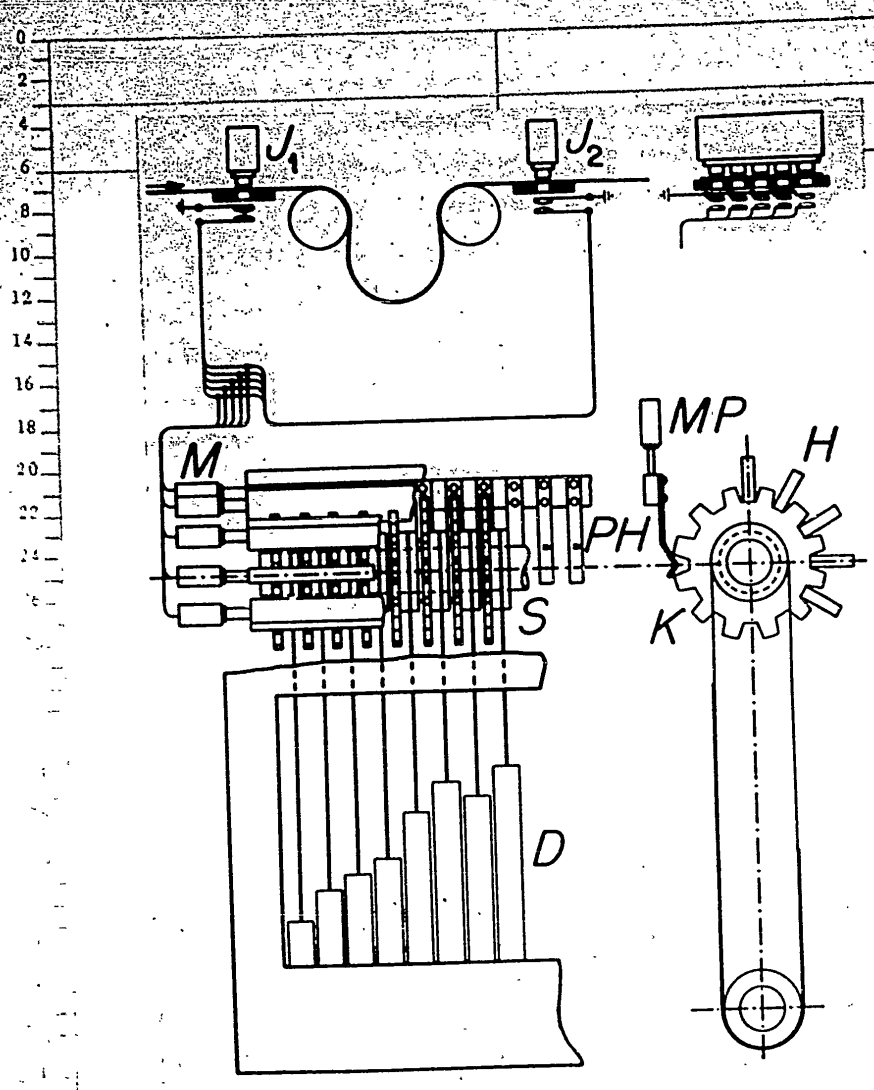

Fig.1 - Scheme of Statistical Analyzer. J_1, J_2 - Reading needles; H - Comb dominating magnet M; S - Saver with wheel K; PH - Strip comb dominated by magnet MP; D - Strips of histogram

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of the (h - n)th element. At this the histogram is changed in such a way that the frequency of the mark corresponding to the hth element is increased by one element and the frequency of the mark corresponding to the (h - n)th mark decreased by one element. The increase or decrease in the frequency is expressed in such a way that the corresponding strip of the histogram is moved up or down by one graduation. After the needles have read the mark, the tape moves forward underneath both sets by one line, so that the first set of needles now reads the mark of the (h + 1)th element and the second set reads the mark of the (h - n + 1)th element. The extent of the investigated collection is therefore always constant.

The composition of the first picture occurs in such a way that the first n elements of the mark of the fundamental collection are read only by the first set of needles. After reading the nth mark, the mark of the first element is displaced underneath the second needles, by which the machine is prepared for the formation of the next picture. The extent of the investigated collection n is therefore equal to the number of elements present between the two sets of needles, and is only limited by the size of the rectangular field.

Actually, the marks of all of the elements in the order of their ascertainment are always perforated in the perforated tape, which enables the reproduction of the observed phenomena. At this reproduction, a new value n can be selected. This characteristic of the machine enables the study of these phenomena at various extents of the investigated collection.

The working speed of the machine is about 3 pictures per second. For simultaneous measurement and perforation of the corresponding mark in the tape the machine can be adjusted in such a way it stops until the signal that the next mark is perforated.

The machine is small, simple and light.

3. Description of Machine. The machine has the following parts (Fig.1): the [illegible] of needles J_1 and J_2, the magnet M, the comb H, the saver S with the

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wheel K, the stripe D, the strip comb PH with the magnet MP, and the rectangular window for observing the histogram.

Both sets of needles J_1 and J_2 move in the openings in the perforated tape and palpate the corresponding combination of perforations. After reading this combination the needles move out and the tape passes underneath the sets by one element forward. Between the needles J_1 and J_2, n elements are present, which determine the extent of the investigated collection of which the histogram is composed.

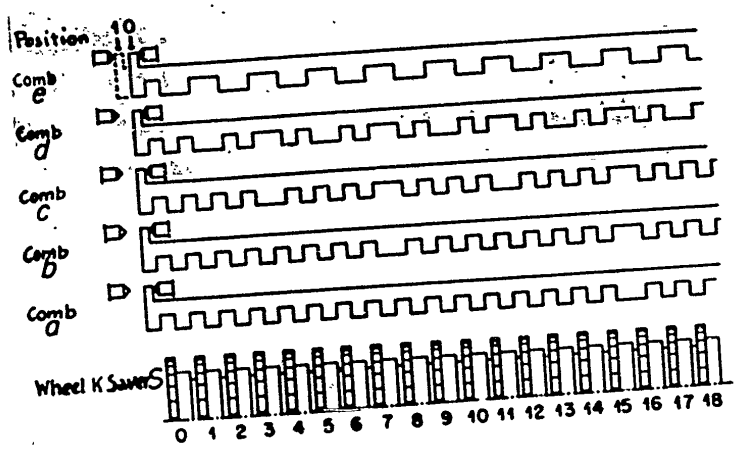

Fig.2 - Example of Execution of Combs. For the combination of combs abcde = 00100 the wheel K_4 is released; for abcde = 00101 the wheel K_5 is released

There are five magnets M for dominating the position of the five combs (Fig.2). Their mutual positions form 25 = 32 different combinations (variations with repetitions). They are made in such a way that they fall into the 32 wheels K of the saver S; at the palpation of one combination of perforations one of these wheels is released which remains standing in its position of the comb.

The magnet MP dominates the strip comb PH, whose strips fall simultaneously

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into the teeth of all of the wheels K of the saver. At disengagement of the magnet MP the whole strip comb is displaced downward , which displaces one tooth forward the wheel K which has been released in the prevailing combination of positions of the combs. The remaining wheels of the saver, which is closed in this combination of positions of the combs, remain standing, because their springs spring out of their catches, and only slide in the corresponding teeth. At engagement of the magnet MP another wheel K is rotated with selection of another set combination of the combs, i.e., one tooth backward. Disengagement of the magnet MP corresponds to the addition of an element to the corresponding frequency of the histogram and engagement to subtraction.

To each wheel K of the saver S one strip of the histogram D is assigned. Therefore by the amount that the wheel is rotated forward, the corresponding strip is moved downward from its fundamental position.

The histogram is observed in a window of dimensions about 10 × 15 cm.

4. Mode of Operation of Machine. Figure 3 shows the time diagram of the machin in which the sequence of the events in the machine is indicated. To it there belong Fig.4 which represents the pulses of the machine. Each is formed in the generator of pulses by one cam. The arrival of the pulses in the machine and the blocked scheme of the whole machine are represented in Fig.5. The working cycle according to Fig.3 is as follows:

1. The needle J_1 engages in the perforated tape.

2. According to the existing combination of perforations are set by means of the magnets M the combs H, which release the wheels, whose sequence on the axle of the saver S corresponds to the combination perforated in the tape.

3. The magnet MP is disengaged, through which the wheel released thereby is rotated by means of the elastic comb one tooth forward, through which the corresponding strip D is displaced one graduation upward (an element is added).

4. The needle J_1 is disengaged and the needle J_2 is engaged.

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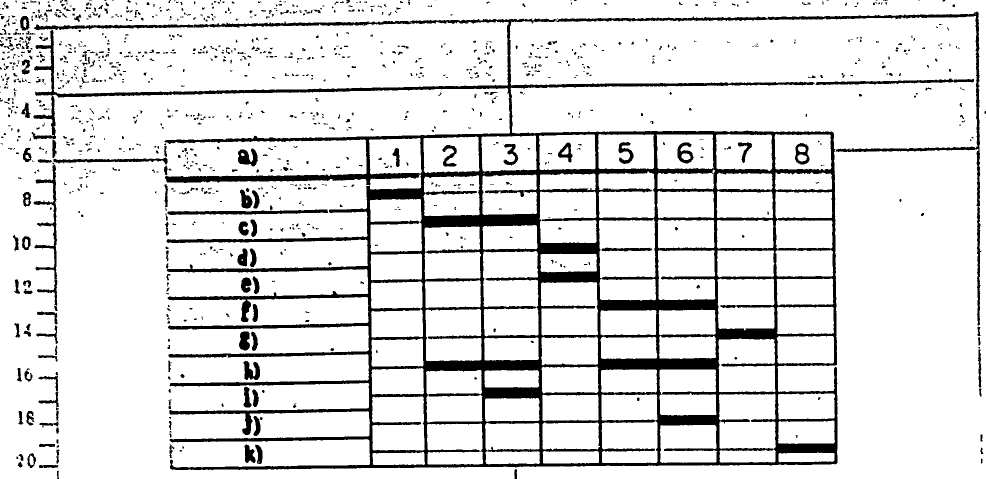

Fig.3 - Time Diagram of Machine. Expressed in eight periods of the sequence of the events in the machine

a) Period; b) Engagement of needle J_1, c) Reading by needle J_1; d) Disengagement of needle J_1; e) Engagement of needle J_2; f) Reading by needle J_2; g) Disengagement of needle J_2; h) Setting of combs; i) Attraction of magnet MP; j) Falling-off of magnet MP; k) Step of tape forward

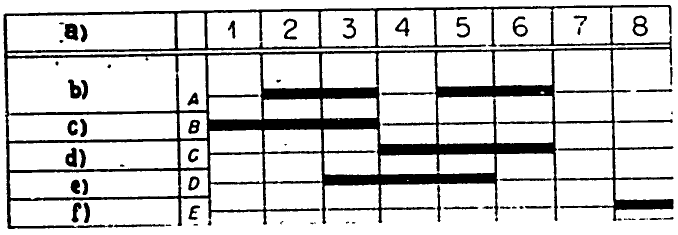

Fig.4 - Diagram of Pulses. (For representation of pulses necessary for proper operation of machine see Fig.5)

a) Period; b) Reading of needles and setting of combs; c) Needle J_1; d) Needle J_1; e) Magnet MP; f) Step of tape;

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5. According to combination of perforations below the needle J_2 the combs are set in a new position, through which is released the wheel corresponding to this new combination of perforations.

6. The magnet is engaged and rotates this newly-released wheel, whose sequence on the axle of the saver corresponds to the combination of perforations in the tape, one tooth backward. By this the corresponding strip is displaced one graduation downward (new value with subtraction).

7. The needle J_2 is disengaged.

8. The tape with the perforated values is displaced one element further.

5. Employment of Machine. For the verification of a hypothesis by the analysis of a phenomenon, experimentally-measured values are frequently processed. The larger the number of the employed values is, the more reliable is the acceptance or rejection of the hypothesis on the basis of the processed information. With the described analyzer the first phase of the statistical processing of such phenomena can be facilitated. The work connection with the condensation of experimental data is mechanical and tedious, and frequently the processing of extensive collections is omitted even to the detriment of the quality of the obtained information and for no other reason.

The expression of the frequencies of the marks of a collection with an extent of n elements is called the concentration of the data. The histogram furnishes a graphic picture of the frequencies of the various marks and their group distribution. The group distribution facilitates the observation of some constant which is characteristic of the observed collection. Such constants are, for example, the mode (most frequent mark), the variable range, etc.

The statistical analyzer may be employed for:

1. The analysis of processes of various kinds.

2. The study of the characteristics of phenomena.

Possible employments of the analyzer are the following:

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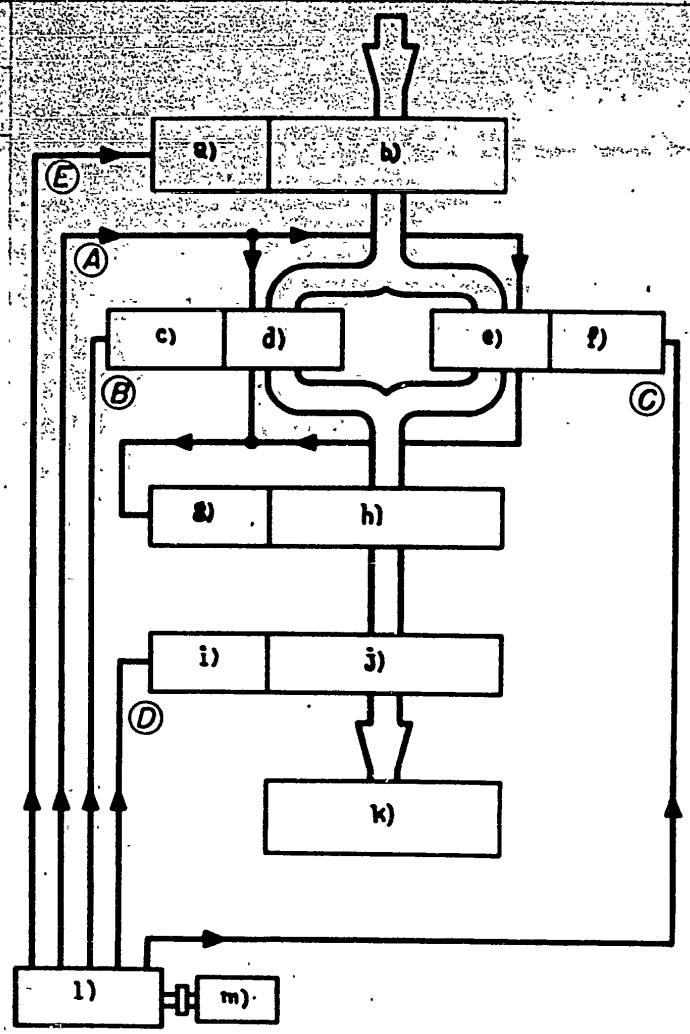

Fig.5 - Blocked Scheme of Machine. Double lines indicate arrival of information in machine. Single lines indicate arrival of pulses from generator of pulses

a) Displacement of perforated tape; b) Tape with perforated values; c) Engagement of needle K_1; d) Needle J_1; e) Needle J_2; f) Engagement of needle J_2; g) Comb magnets M; h) Combs H; i) Displacement of wheels of saver; i) Saver S; k) Histogram k; l) Generator of impulses; m) motor

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1. For the complete investigation of all formed pictures;

2. For the reproduction of the same observation at various selected extents of the investigated collection n;

3. For the intermittent study of the phenomena in a picture formed from n elements, i.e., in such a way that the machine is stopped at every k^{th} formed picture (where $k \leq n$).

The phenomena whose study can be facilitated by the employment of the statistical analyzer occurs in various sciences (geophysics, aerodynamics, etc) as well as in various technologies (at the investigation of the stability of products, especially at quality verifications by measurement). Thus, for example, by the employment of the analyzer in connection with a production process, the magnitude and the character of the changes which do not transgress the tolerated limits can be investigated. There is a possibility of investigating a production process or of observing the occurrence of systematic errors not yet perceptibly manifested in the finished product (for example, at changes in the adjustment of machines, the dulling of knives, etc).

The described statistical analyzer is designed in such a way as to carry out only the fundamental functions necessary for investigating the concerned phenomena according to the given method. However, this model can fairly easily be supplemented with a number of simple attachments.

By suitable arrangements it has easily been possible to construct the picture of a histogram in which the transgression of the phenomena was not observed (setting of the upper and lower limits in which the frequencies of the individual marks may vary). At their transgression the machine gives a suitable optical or acoustical signal, etc.

By introducing into the machine two perforated tapes (each of which served for registration of the same phenomena under different conditions), in such a way that the one tape was palpated by the one needle and the other tape by the other needle,

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it was possible to carry out the comparing analysis of these two phenomena. The employment of the analyzer for such a purpose requires small adjustments of the machine, and displacement of the strips in the rectangular field in such a way as to make contact in the fundamental position with the zero line in the middle of the rectangular field.

If the investigated phenomenon is periodical, and if n just equals the period, then the picture investigated with the analyzer no longer changes. (The element of the same mark which is added is also immediately subtracted, so that all of the pictures are always the same.) If n does not equal the period, the phenomenon of the particular character changes the picture.

The analyzer could be further developed for the simultaneous ascertainment or registration of a characteristic constant of the investigated collection, for example, the arithmetic average, the mode, the dispersion, etc.

The proper employment and adjustment or adaptation of the statistical analyzer requires before all thorough knowledge of the corresponding fields. It is now up to the scientific and technological workers to consider further possibilities of concrete applications.

Remark: This article, under the title of "Machine for Investigation of Histograms of Frequencies" was submitted to Slaboproudy obzor (Weak-current Survey) on September 8, 1953, by whom it was returned on October 26, 1953 because it did not seem to fit into the editorial policy of this journal

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SUMMARY

The statistical analyzer is a machine for facilitating the statistical study of phenomena. In following such phenomena, their distribution histogram is [illegible]ed

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on a rectangular field by means of perpendicular dark stripe.

The histogram is established for n elements of the basic collection. The machine constantly adjusts the histograms in that for each k-th element added to the appropriate magnitude in the distribution, it subtracts from the appropriate magnitude one unit for the (k + n)-th element. The machine is thus particularly suitable for the study of phenomena whose properties depend on the order of the elements.

After describing the machine and its mode of operation, the authors present several possible applications for the machine as well as other possible designs and extensions.

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SYNTHESIS OF TEN-JOINT MECHANISM AS GENERATOR OF FUNCTIONS OF THREE-INDEPENDENT VARIABLES

by

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1. Joint Mechanism with Several Degrees of Freedom

1.1 Introduction. In this article we wish to describe a graphic method for the synthesis of a ten-joint mechanism with three degrees of freedom. We wish to describe it in such a way that for its final refinement, after verification with reference to the example presented in the last chapter, and after the addition of several methodical artifices, the method can be supplemented on the basis of studies carried out later. The given problem is still far from being completely solved. Its difficulty is of such a nature that the creation of the theoretical basis for its solution is sufficient for the preliminary construction of the fundamental knowledge. Specifically, it is the introduced concept of the network function and mechanism which is the center of interest of this work. All that remains therefore is to define the most important concepts. For the description of the method the concept of the network will be employed for the synthesis of a ten-joint mechanism with three degrees of freedom. At the same time some fundamental methodical artifices will be described.

Accordingly we shall not attempt to define the range of the functions depicting the ten-joint mechanism. We shall be satisfied with the assumption that the ten-joint mechanism is depicted with sufficient precision by the given functions. We assume further that the given functions do not have any relative extremes, although the ten-joint can also be depicted by such functions without particular difficulties.

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Finally, we hope that no confusion will result from the fact that we employ comparatively (but not explicitly) defined concepts. This is the case where a precise definition would require a corresponding digression from the actual work and when the context itself is a sufficient explanation of the employed concept.

1.2 Synthesis of Joint Mechanisms with Several Degrees of Freedom. The synthesis of joint mechanisms with several degrees of freedom is difficult, especially for four reasons:

1. By the given functions the mechanism can usually be created only approximately (but in the limits of the required precision). This approximation is due to

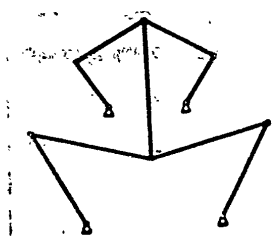

Fig.1 - Frog Mechanism. This is the ten-joint mechanism with three degrees of freedom whose synthesis is described in this work

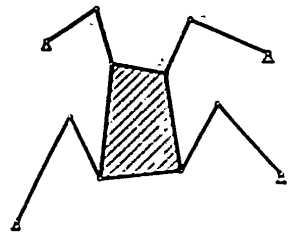

Fig.2 - Spider Mechanism. This is an example of a type of link mechanism with three degress of freedom for which a method of synthesis has not been worked out

the fact that for the creation of the functions we employ a mechanism of a predetermined type, which creates ranges of functions which the given functions do not contain precisely. This imprecision cannot be eliminated afterward by precise execution of the mechanism.

2. A joint mechanism has a large number of variable parameters, which represent unknown magnitudes of the problem.

3. Because of 1, it is usually possible to find several different,

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approximate solutions. However, the parameters of the mechanism representing this solution may differ considerably from each other.

4. The functions of two variables are depicted graphically by a curve, the functions of three variables by a system of curves in a plane. For the representation of the functions of four variables it is necessary to depict a spatial system of planes. Our work is therefore complicated by the fact that with the graphic method a simple method for planar representation of the functions of four variables is lacking.

The procedure at the synthesis of a joint mechanism usually consists in seeking with the help of a suitable graphic method the mechanism which creates the given functions at least approximately. At this the formative parameters are improved until the employed graphic method is sufficiently precise. In this way we get a formulation of the mechanism which serves as the basis for further solution by the numerical method.

The method which we introduce is a graphic method for the synthesis of a ten-joint mechanism with three degrees of freedom, the so-called frog mechanism (Fig.1), suitable for the formation of three independent variables. For its formulation we start with the given functions, which are suitably tabulated. For its representation we introduce the concept of its reticularity. The reticularity of a function is the fundamental characteristic of the function which enables its employment for the synthesis of link mechanisms with three degrees of freedom, also when they are of a type other than that assumed in this work (for example, the "spider mechanism" of Fig.2). It can also be employed for the synthesis of mechanism which are not purely link mechanisms, as well as for the synthesis of mechanisms with degrees of freedom other than those of the type described here. However, the corresponding methods have not yet been worked out. The graphic method of formulation usually leads to a mechanism which is not formed by the given functions with the required precision. However, the mechanism in this form usually differs so little from a satisfactory

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mechanism that it can be further refined by the employment of one or another known numerical method, which are not described in this work.

The graphic part of the formulation of a ten-joint mechanism represents the difficult part of the synthesis. Moreover, the work carried out so far is only a fraction of the whole work.

2. Concepts and Definitions

2.1 Homogeneous Variables. For the representation of the functions of four variables of a link mechanism, we introduce with advantage instead of the given variable the so-called "homogeneous variable", defined as follows:

$$h_n = \frac{x_n - x_{n\,min}}{x_{n\,max} - x_{n\,min}}; \quad n = 1, 2, 3, 4;$$

where x_n is the variable defined in the interval $x_{n\,min} \leq x_n \leq x_{n\,max}$.

At the search for a suitable link generator of the function $f(x_1, x_2, x_3) = x_4$ it is attempted to find a mechanism which can be precisely depicted by the given functions for 5^3 values of the dependent variables. The corresponding values of the independent variables are selected with the help of the indices i, j, k, which are assigned to the values of the independent variables according to the following Table:

Homogeneous variable	h_1	h_2	h_3		
Corresponding index	i	j	k		
Value of homogeneous variable	0.00	0.025	0.50	1.75	1.00
Value of corresponding index	1	2	3	4	5

2.2 Network of Independent Variables. The points of the network of the independent variables are called the triplet of values of the independent variables corresponding to the triplet of indices, in which the first index i belong the first independent variable, the second index j belongs to the second independent variable and the third index k belongs to the third independent variable. When we have in mind the points of the network, we write the triplets of these values or the trip-

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lets of these indices in the formula. For example, (i, j, k) = (3, 1, 4) means the points of the network for which $h_1 = 0.50$; $h_2 = 0.00$; $h_3 = 0.75$.

The network of independent variables is the set of all of the thus-defined points of the network of the independent variables. There are $5^3 = 125$ points.

2.3 Values of Point of Network of Independent Variables. The values of the points of the network (i, j, k) are the values of the dependent variables corresponding to the values of the independent variables in these points. They are usually expressed by the values of the homogeneous variable h_4.

2.4 Reticularity of Functions. The functional problem $f(x_1, x_2, x_3) = x_4$ assigns to each of the points of the network its value. If we arrange the points of the network according to the magnitudes of their value h_4, we get an arrangement of the triplets (i, j, k) which is characteristic of the given function (with the given interval of the independent variables). If there are several points of the network with the same value, they belong in the same place in this arrangement.

The reticularity of a function is a characteristic property of the function given by the arrangement of the points of the network according to the magnitudes of its value.

3. Analysis of Ten-Link Mechanism with Three Degrees of Freedom

3.1 Nomenclature of Members of Mechanism (Fig.3).

Input cranks	V_I, V_J, V_K
Output crank	V_V
Scales of input variables	S_I, S_J, S_K
Scales of output variables	S_V
Draw-rod of output variables	T_I, T_J, T_K
Draw-rod of input variables	T_V
Middle draw-rod	T_S

3.2 Formative Parameters. The ten-link mechanism has 19 formative parameters, as follows: the lengths of the four cranks, the lengths of the four draw-rods, the

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length of the middle draw-rod, the three angles for the zero positions of the input cranks, the three angles expressing the working range of the independent variables,

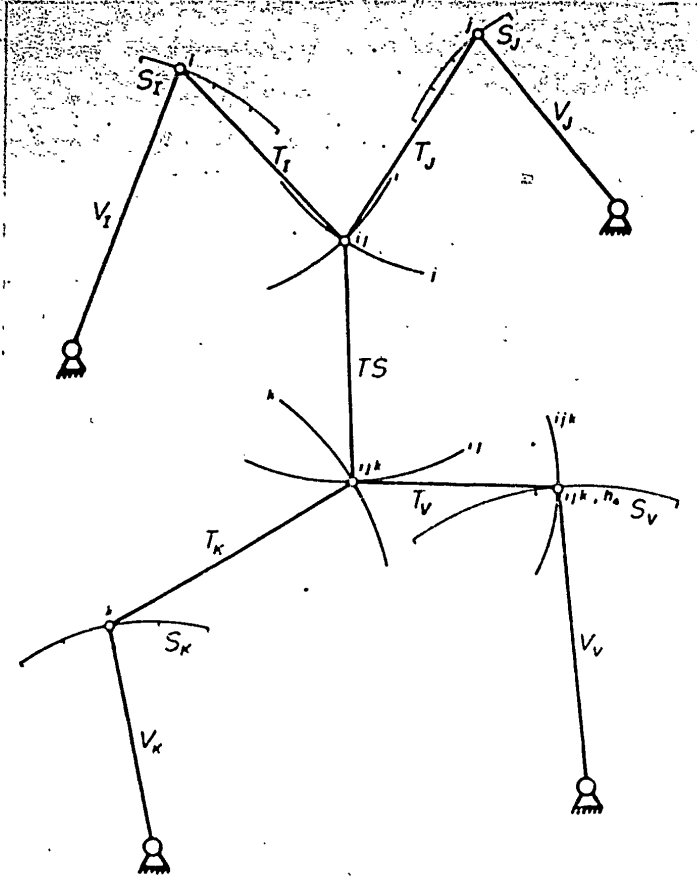

Fig.3 - Nomenclature of Members of Ten-link Mechanism

and the four coordinates of two fixed links. Assuming inequality of the divisions of the scales of the variables, we add to these fundamental parameters the further formative parameters.

A small change in a formative parameter has a small influence on the reticular-

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ity of the formative functions of the mechanism. If we carry out such a change of a formative parameter (small or finite) which has no influence on the reticularity of the formative functions, we actually have two different mechanisms. The reticularity of both of the functions which form these two mechanisms is the same. In this sense we regard these two mechanisms as equivalent (see Chapter 5).

3.3 Representation of Functions of Ten-Link Mechanisms. A ten-link mechanism which forms the function $F(x_1, x_2, x_3) = x_4$ is given. Its input scales are denoted by the corresponding values of the indices i, j, k.

The input cranks V_I, V_J, V_K are set up on the scales S_I, S_J, S_K of the independent variables on the values corresponding to the indices i, j, k, by which we have selected the points of the network (i, j, k). At this the input cranks are set up in such a way that on the input scales we read the values of the selected points of the network. The formative function $F(x_1, x_2, x_3) = x_4$ may therefore be regarded as follows: by setting up the input cranks on the points corresponding to indices i, j, k on the input scales, we select the points of the network. To the output scale of the mechanism, the values of the selected points of the network are assigned. The arrangement of the points of the network on the output scale therefore expresses the characteristic of the function which we call the reticularity.

For the given function $f(x_1, x_2, x_3) = x_4$ and the function $F(x_1, x_2, x_3) = x_4$ of the formative mechanism therefore the following important statement is valid:

If the function $f(x_1, x_2, x_3) = x_4$ has the same reticularity as the function $F(x_1, x_2, x_3) = x_4$ of the formative mechanism, then this mechanism can be precisely depicted by the function $f(x_1, x_2, x_3) = x_4$ for all of the points of the network.

3.4 Analysis of the Formative Functions of the Mechanism. Definition of the field of the point E_{ijk} and the field D_{ij}. The input cranks V_I, V_J, V_K describe with their free ends the curvatures of the input scales S_I, S_J, S_K. The output crank V_V describes with its free end the curvature of the output scale S_V. On the output scales the points 1, 2, 3, 4, 5 corresponding to the values of the respective

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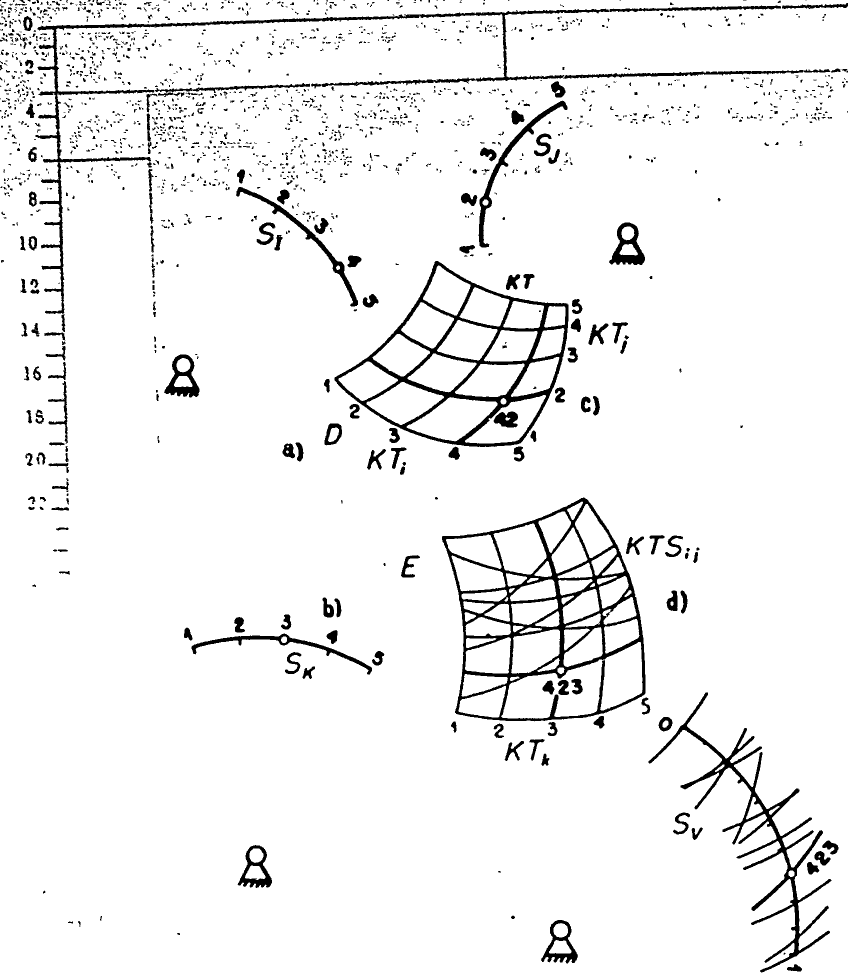

Fig.4 - Analysis of Structure of Ten-Link Mechanism

a) Region D; b) Region E; c) Field of point $D_{i,j}$;

d) Field of point $E_{i,j,k}$

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indices (Fig.4) are denoted.

The draw-rod T_I describes similarly from the center on S_I ($i = 1, 2, 3, 4, 5$) the five curvatures of the draw-rod T_I. These curvatures are denoted KT_i. Each of the curvatures is denoted by the index of its center.

The draw-rod T_J describes with the center on S_J ($j = 1, 2, 3, 4, 5$) the five curvatures of the draw-rod T_J. These curvatures are called KT_j. Each of the curvatures is denoted by the index of its center.

Each of the pairs of curvatures, one of which is described by the draw-rod T_I and the other by the draw-rod T_J, has two intersections. Unambiguity of the formed function requires that one of them be excluded. When the mechanism passes through all of its working positions (i.e., all of the positions in which it depicts the functional relation), the common link of the draw-rods T_I and T_J is displaced into the region which we call the region D. To this region belong all of the nonexcluded intersections of the curvatures described by the draw-rods T_I and T_J.

The intersection D_{ij} of the curvatures VT_i and KT_j (in the region D) is denoted by a pair of indices, of which the first corresponds to the index of the curvature KT_i and the other to the index of the curvature KT_j. Such a set of points, arranged according to the indices i, j, is called the field of the point D_{ij}.

When the mechanism passes through all of its working positions, the common link of the central draw-rod T_s and the draw-rod T_k is displaced into the region which is called the region E. The common link mentioned describes curves about the point D_{ij}. Each of these curves is denoted by a pair of indices corresponding to the pair of indices of its center. The arc of this 25th curve of the central draw-rod present in the region E is called KTS_{ij}.

The draw-rod T_K describes with the center ($k = 1, 2, 3, 4, 5$), the scale S_K of the five curves of the draw-rod T_K. Each of the curves is provided with the index of its center. These five curves KT_k form with the curves of the central draw-rod $5 \times 5^2 = 125$ intersections present in the region E. Each of the intersections

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is denoted by a triple index. The first two indices of this triplet form in the indices i, j, belonging to the curves of the central draw-rod, and the third index of the triplet forms the index belonging to the curve of the draw-rod KT_k. These intersections E_{ijk} form a set of points arranged according to the indices i, j, k. This set is called the field of the points E_{ijk}.

The draw-rod T_V describes with the points E_{ijk} as centers 125 curves of the draw-rod T_V. These curves are called KT_V. Each of them is denoted by the triplet of indices of its center. These curves intersect the scale S_V in 125 points. Each of them receives the triplet of indices i, j, k corresponding to the individual points of the network (i, j, k). These points are arranged on the output scale according to increasing value h along the scale S_V. Their arrangement is predetermined by the reticularity of the given mechanism.

3.5 Characteristics of Field of Points E_{ijk}. The field of the points E_{ijk} contains 125 points E_{ijk}. If we put in succession k = 1, 2, 3, 4, 5, the field is divided into five groups E_{ijk} (k = const) of 25 points each lying on the same curve KT_k.

The field of the points E_{ijk} can also be divided into 25 groups of five points each lying on the same curve KTS_{ij} by putting in succession i, j = 00, 01, ... 54,55, These are groups of E_{ijk} (i, j = const).

3.6 Curves of Central Draw-rod KTS_{ij}. The curves of the central draw-rod KTS_{ij} (i, j = const) are defined by their centers present in the field of points D_{ij}. However, for the pair of indices given they can also be defined with the help of the points E_{ijk} (i, j = const). Let us see how these points can be constructed.

In paragraph 3.4 we found that the points E_{ijk} (i, j = const) correspond on the scale S_V to five intersections of the scale with the curves described about these points by the radii of equal length of the output draw-rod and hence also to five values of the points expressed by the homogeneous variable h_4. Here, on the contrary, we start with five given points of the network (i, j, k) (k = const) and

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their values h_4, and seek the corresponding points E_{ijk} (i, j = const) in the range E.

From the corresponding points on the scale S_V (according to h_4) we describe with the radii of equal length of the output draw-rod T_V the arc traversing the

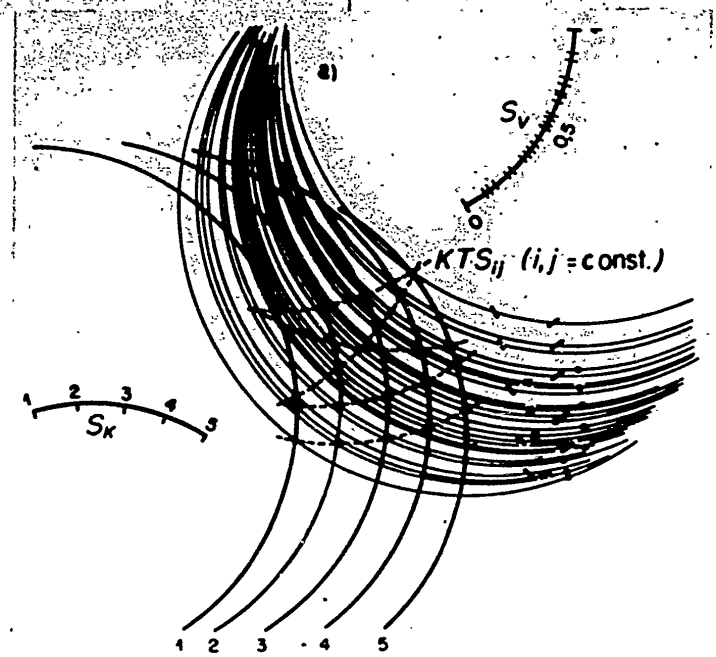

Fig.5 - Construction of Five Curves of Central Draw-Rod KTS_{ij} (i, j, = = const) with Help of Curve KT_k, Output Scale S_V and Known Length of Draw-Rod T_V

a) Color curves

region E and denote it by the index k (according to the corresponding triplet of indices i, j, k). Further we describe the five curves KT_k from the index S_k with the radii of equal length of the draw-rod T_K. The curves of the same index k form in the region E five intersections E_{ijk} (i, j = const), which lie on the curve KTS_{ij}.

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The points E_{ijk} (k = const) at the same time define the points D_{ij} as the centers of the curves given by these points.

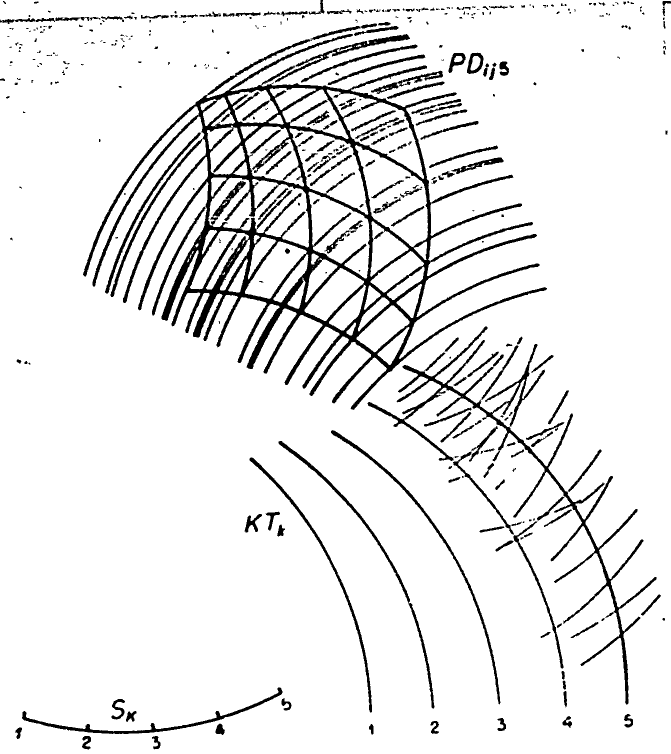

Fig.6 - Field of Points D_{ij} Bounded by Curves Described from Point E_{ij5} of Region E with Radii of Equal Length TS. Called PD_{ij5}

3.7 Color Curves. We select five sets of points of the network

$$(1, 1, k),\ (1, 5, k),\ (3, 3, k),\ (5, 1, k),\ (5, 5, k).$$

To each of the sets we assign one color. We select one of these sets and seek on the output scale S_V the point corresponding to the value h_4 of the point of the network of this set. From the point on the scale, we describe the curves radii

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of equal length of the output draw-rod T_V to which the color belongs. The curves are denoted with the index k. We do this in succession for all five of the selected sets.

The curves corresponding points (i, j, k) (i, j = const), whose centers lie in the corresponding points on the output scale S_V, and on which is clearly indicated (for example, by colors) which five correspond to one and the same set (i, j, k) (i, j = const), are called color curves. The curves belonging to these sets of points (i, j, k) (i, j = const) are called curves of the same color. The colors are then provided with the index i, j.

We intersect the curves of the same color with the curves KT_k. Of the intersections lying in the region E, we are interested only in those formed by the intersection of the curves of the same index k. In this way we get five points of the particular curve KTS_{ij} (Fig.5).

3.8 Characteristics of Field of Points D_{ij}. We select in the region E the points E_{ijk} for the selected k = const. We described from them the curves with radii of equal length of the central draw-rods T_S in such a way that they pass through the region D. Each of these curves passes through at least one point D_{ij}. The indices i, j of the points D_{ij} and the centers E_{ijk} of the described curves are in agreement with each other (Fig.6).

All of the points of the sets E_{ijk} (k = const) lying on the arcs of the curves KT_k delimit the region E. Therefore any of the points E_{ijk} of these sets divides the points lying on these arcs into three groups:

1. The points lying on the one side of the selected point;
2. The points lying on the other side of the selected point;
3. The points coinciding with the selected point.

The curves described by this selected point in the manner described above divide all of the points D_{ij} into three groups, which correspond to the above-mentioned groups. These are:

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1. The points lying on the one side of the described curve;

2. The points lying on the other side of the described curve;

3. The points coinciding with the described curve.

There are 25 curves described from the point E_{ijk} (k = const), and we call them KD_{ijk} (k = const). Because the point D_{ij} and the curve KD_{ijk} (k = const) form in the plane of the mechanism the geometrical form with which we have to operate, we introduce for it a special term, "field PD_{ijk}" (k = const).

4. Synthesis

4.1 Formulation of Problem of Synthesis of Link Mechanism. The function $f(x_1, x_2, x_3) = x_4$ is given. We have to design a ten-link mechanism which forms the function $F(x_1, x_2, x_3) = x_4$ in such a way that

$$f(x_1, x_2, x_3) - F(x_1, x_2, x_3) < \varepsilon .$$

where ε is the required precision.

In view of the method of designing this mechanism, we formulate this problem as follows:

We have to determine the formative parameters of the ten-link mechanism in such a way that the reticularity of the function $F(x_1, x_2, x_3) = x_4$ corresponds as well as possible with the reticularity of the function $f(x_1, x_2, x_3) = x_4$. Therefore, for improving this designed mechanism in such a way as to satisfy more precisely the requirement

$$f(x_1, x_2, x_3) - F(x_1, x_2, x_3) < \varepsilon .$$

there is further necessary the application of a numerical method.

4.2 Introduction to Method. The problem of the graphic stage of the designing of a link mechanism consists in the designing of a mechanism which will depict the given function sufficiently precisely. The first graphic construction gives a mechanism which exhibits considerable deviations but constitutes a suitable basis

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for processing, leading to improvement of the mechanism. In this way we get a second design of the mechanism. Its parameters are again used as the starting values for working out the next design. We continue in this way until we have a sufficient precision of the graphic construction.

We begin the first design of the mechanism with the designing of the output scale S_V. Its radii are at first selected wholly arbitrarily. We operate well with a radius equal to about 10 cm. The arc of the scale is selected at 60° to 90°. The graduation of the scale is in equal intervals from 0 to 1 (the output scale is always numbered in the values of the homogeneous output variable). At the further synthesis, however, we make no effort whatever to keep this scale uniform. The permissibility of making the scale uneven greatly facilitates the synthesis. In view of the fact that with a four-link mechanism (Bibl.1) a nonuniform scale can easily be transformed into a uniform scale, we regard it as wasted to insist on a uniform graduation of the output scale at any price. However, this does not mean that we neglect the opportunity of attaining a uniform graduation of the output scale during the whole graphic process.

The second step in the synthesis is the designing of the scale S_K. The radius of the scale is again selected at about 10 cm, its arc at about 60° to 90°. In contrast to the scale S_V we have marked on this scale only five points, corresponding to the values 1, 2, 3, 4, 5 of the index k. The scale S_K is at first selected uniform. Each of its five points can be displaced along the scale as required at the further processing. In this way a uniform graduation of the scale S_K can be obtained. This facilitates the synthesis of the mechanism, because the possibility of employing a nonuniform graduation of the scale enormously extends the range of the function depicted by our ten-line mechanism.

With the help of the scales S_V and S_K, we design the field of points E_{ijk} (see Figs. 3 and 4). When we have finished with its designing, (even only very approximately) we already know some of the formative parameters to which there belong the

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radii of the scales S_V, S_K, the problem of the extent of these scales and the lengths of the draw-rods T_V and T_K, as well as the parameter determining the relative positions of the scales.

With the help of the field of points E_{ijk} and a suitable selection of the length of the central draw-rod, we derive the field of points D_{ij}, which serves as the basis for the approximate formulation of the parameters V_I, V_J, and T_I, T_J, as well as for the formulation of the relative positions and the graduations of the scales S_I and S_J.

Then the whole procedure is reversed. With the help of the last-obtained parameters we construct the field of points D_{ij}, which, especially in the beginning, differs considerably from the field of points D_{ij} derived from the field of points E_{ijk}. We adjust the field of points D_{ij}, at which we obtain in succession better and better values of the last-mentioned parameters. With the help of the adjusted field of points D_{ij}, we design the curve KT_k and construct a new field of points E_{ijk}. Then with the help of the field of points E_{ijk}, we design a new output scale S_V.

The individual steps of this designing are described in detail in the next paragraph.

4.3 Arrangement of Functions before Beginning Search for Mechanism. We introduce to the given function a homogeneous variable. For all of the points of the network we calculate the value of this function. We take 125 blank cardboard sheets. For each of the points of the network we take one sheet, and inscribe it as follows:

i	j
k	h_4

where i, j, k are the indices of the triplet of indices of the points of the network, h_4 is the value of the corresponding point of the network. The sheets form a pack B.

4.4 Plotting of the Color Curves. We draw on paper a uniform output scale S_V. Its dimensions are at first selected at random. From the pack B we select the sheets

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corresponding to the points of the network

$$(1, 1, k), (1, 5, k), (3, 3, k), (5, 1, k), (5, 5, k),$$

where k = 1, 2, 3, 4, 5. Five of these sheets which have the same index i, j always belong to the same curve of the central draw-rod, i.e., the curve KTS_{ij}.

We select five colors of ink. With the first color we describe five semicircles with a suitable (at first arbitrary) selection of the radius of the scale S_V. Their centers are placed according to the corresponding values of h_4 written on the sheets (1, 1, k).

The center of the curve drawn with the second color is placed according to the corresponding value of h_4 on the sheet (1, 5, k) etc. until the center of the curve drawn with the last color is placed according to the corresponding value of h_4 on the sheet (5, 5, k). All of these color curves are denoted by the corresponding index k.

4.5 Designing of Field of Points E_{ijk}. We draw on transparent paper, with a radius selected arbitrarily (at first, for example, the same as the radius of the scale S_V), the scale S_K. On it we select five equidistant points, which we denote by the index k. The arc of the scale S_K formed in this way corresponds to about $\frac{1}{4}$ the circumference of the circle. From these points we describe with India ink five curves (best filled) corresponding to the curve KT_k. We denote them by the index k.

Here the transparent, which we shall call the transparent R, is laid on the drawing with the color curves. We distinguish the first color the transparent of the curve from the curve KT_k, whose transparent has the same index k. These five intersections are joined by hand to a smooth line, and named the index 11. This line also corresponds to the curve 11 of the central draw-rod, i.e., the curve KTS_{11}.

In the same way we join five such intersections of the curve of the second color with the curve KT_k. This gives a line corresponding to the curve KTS_{15}. We do this in succession for all of the color curves. The lines are indexed 15, 33, 51, 55.

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We have obtained five lines, which have to be curves of the central draw-rod, i.e., ideally have to be curves of the same radius. Then we determine by inspection which of the parameters so far selected have to be changed and how much to give curves of the same radius. These changes may be:

1. Change in the relative positions of the transparent and the paper;

2. Changes on the transparents R (radii of the curves KT_k, clearance between curves KT_k, radius of the scale, graduation of the scale);

3. Changes on the drawing (graduation of scales, radii).

For change 1 it is sufficient to re-draw the sketched five lines. Change 2 requires re-drawing of the transparent R. Change 3, for practical reasons, is not considered until after we have exhausted the remaining possibilities. After making the changes in the corresponding parameters, we begin again with the selection of the field of points E_{ijk}. After obtaining the five new lines corresponding to the five curves KTS_{ij}, we proceed further as before. If we are again unsatisfied with the result, we formulate still another field of points E_{ijk}. We continue to do this until the five lines obtained resemble as well as possible curves with the same radius.

We succeeded with the first design of the scales S_K and S_V in formulating their relative positions and the lengths of T_K and T_V. The parameters thus obtained determine the field of points E_{ijk} in the form of the field of the intersections of the curves whose radii equal the lengths of the formulated draw-rods T_K and T_V described from the corresponding points of the scales S_K and S_V.

4.6 Formulation of Field of Points D_{ij}. According to the best parameters formulated so far (magnitudes of radii, relative positions and graduations of scales S_V and S_K), we draw the curves KT_k and the scale S_V on the same drawing. With the help of the pack B we construct in succession all 25 of the lines corresponding to the curves of the central draw-rod KTS_{ij}. These lines we shall call the lines KTS'_{ij}.

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The centers of the curves of the central draw-rod form the field of points D_{ij}. For being able to determine this field we use a transparent with concentric curves (Fig.7). The transparent is first applied to the line KTS_{ij} for the purpose of ascertaining which of the curves matches this line the best of all. The found curve is noted on the transparent. The marked curve of the transparent is again applied to all of the lines KTS_{ij}. At this we always distinguish the positions of the centers of the points which we denote with the index i, j according to the index of the corresponding line. With this we have obtained the first approximate picture of the field of points D_{ij}. It is clear that we cannot determine these centers at all precisely the first time. It is often better to try a whole area

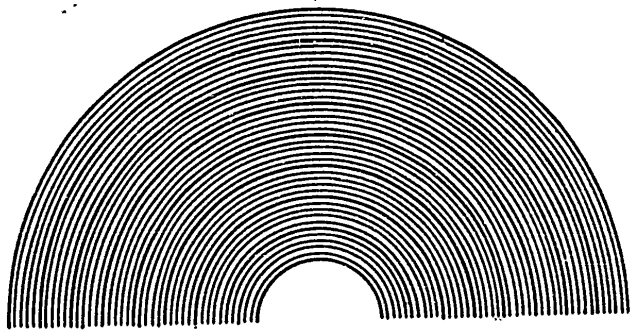

Fig.7 - Transparent with Concentric Curves Suitable as Aid for Determination of Radii of Curves which Come Closest to Those of Lines Drawn by Hand

in which centers might be present.

The points of the field D_{ij} (for example, an area) we join by hand with a line in such a way that we always join the points which have the same first index i and then the points with the same second index j. These two systems of lines correspond to the curves KT_i and KT_j. Since these lines are only approximations of the curves, we shall call them the lines KT_i and KT_j.

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The obtained lines KT'_i and KT'_j serve as the basis for the formulation of the curves KT_i and KT_j. Next we select the radii of the scales S_I and S_J, their graduations, their relative positions, and the lengths of T_I and T_J, and construct the curves KT_i and KT_j. The selection of these parameters is made in such a way that these curves have the same character as the lines KT'_i and KT'_j. At this it is sufficient to plot this character only very approximately. The lines are actually (especially in the beginning) only rough guides for the selection of the considered parameters. At the first formulation of the mechanism the field of points D_{ij} derived from the lines KTS'_{ij} is such that it is scarcely decisive for some of the values of the parameters. Therefore it is best first of all to re-draw the obtained field by hand in order to be able afterward with the help of the transparent with concentric curves more easily to determine the necessary parameters. The redrawn field is thus a special idealized field of the derived field of points D_{ij}.

According to the estimated parameters we draw the curves KT_i and KT_j in a suitable scale and denote their intersections present in the region D with the double index i, j. With this the field of points D_{ij} is formulated.

4.7 Arrangement of Field of Points D_{ij}. The pack B is sorted into five groups of sheets according to the index k. The sheets of each pack are arranged according to magnitudes of the h_4 value of the points of the network. The sheets with the same value of h_4 can be put together in any order. The five packs B_{ijk} (k = const) formed in this way correspond to the set E_{ijk} (k = const) (see paragraphs 3.5 and 6). Every selected sheet of any pack divides it into three groups: a first group containing the selected sheet and every sheet which has an h_4, the same as the selected h_4; and a third group containing the remaining sheets. Each sheet corresponds to the index i, j to one point of the field D_{ij}.

We select several sheets if the pack B_{ijk}. We plot with the corresponding points D_{ij} a line which divides this field of points in a manner similar to that by which the selected sheet divides the sheets of the pack, i.e., a line which

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will pass through the points D_{ij} which belong to the sheets of the above-mentioned first group, at which at the same time divides the region D into two parts, in such a way that in each of the parts there are present points D_{ij} belonging to excluded sheets of the same group. Let this line be for the time being as smooth as possible. Such a line is drawn for all of the sheets of the pack. The region D divided by this line is denoted PD_{ij1}. In this work we continue in succession with the packs B_{ij2} to B_{ij5}. For each of the packs we draw a line to another of the prepared five fields D_{ij}. The obtained pictures are denoted PD_{ij2} to PD_{ij5}.

The lines drawn in all of these fields must be curves of the same radius. Their radius must equal the length of the central draw-rod. The parameters of the curves KT_i and KT_j are changed in succession in such a way that all of these lines resemble as well as possible curves of the same radius. We change the radii of the scales, the lengths of the draw-rods T_I, T_J, the graduations of the scales and their relative positions.

After changing the parameters we repeatedly arrange the field of points D_{ij} until we have a satisfactory result, i.e., until we are no longer able to improve the field of points D_{ij}. In the field of points D_{ij} with which we are finally satisfied, we denote the individual points with the corresponding double index i,j.

4.8 Formulation of Curve KT_k. For obtaining the basis for the formulation of the curve KT_k we use the transparent with concentric curves. With its help we easily find the curve which matches best the line drawn in all five of the fields PD_{ijk} (k = 1, 2, 3, 4, 5). This curve is marked on the transparent. Its radius represents the length of the central draw-rod T_S.

Next we lay this transparent on the field D_{ij1} in such a way that the marked curve matches as well as possible some line drawn in this field, and we mark the position of its center. We do this for all of the lines drawn in the field D_{ij1}. We mark the centers which would ideally be present on the curve KT_k (k = 1), and join them with a line by hand. In the same way we apply the selected curve of

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transparent to the lines in the field PD_{ijk} ($k = 2, 3, 4, 5$) and mark the positions of their centers. The centers derived in these fields are always joined by a line by hand.

With this we have obtained a suitable basis for the selection of the parameters of KT_k and the parameters for determining the relative positions of the curves KT_k and the field of points D_{ij}. With these parameters the field of points E_{ijk} is then determined as the form of the field of intersections of KTS_{ij} and KT_k.

4.9 Formulation of the Output Scale. The pack B is sorted into five groups according to the index j. The sheets of this pack are arranged according to the magnitudes of the h_4 value of the points of the network. The formed five packs B_{ijk} (j = const) correspond to the set of points E_{ijk} (j = const) of the field of points E_{ijk}.

For the formulation of the output scale the pack B could equally well be sorted according to the index i. Decisive for this is the index which is based on the reticularity of the given function. Since, however, the selection of the index is not decisive for the further procedure, we need not consider this matter further here.

Every selected sheet of any pack divides it into three groups: a first group containing the selected sheet and every sheet with the same h_4 as the selected sheet; a second group containing the sheets with a smaller h_4; and a third group containing the remaining sheets. Each of the sheets corresponds according to the indices i, j, k to one point of the field E_{ijk}.

The sheets of the pack B_{ijk} correspond to the point E_{ijk}. The distinguishing of these 25 points in the field of points E_{ijk} is obtained with the help of the parameter mentioned at the end of the next paragraph. We select any sheet of the pack B_{ijk}. We plot with the corresponding points E_{ijk} a line which divides this field of points E_{ijk} in a manner similar to that by which the selected sheet divides the sheets of the pack, i.e., a line which will pass through the points E_{ijk} which

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belonging to the sheets of the above-mentioned first group, and which at the same time divides the points of the field E_{ilk} into two parts, in such a way that points E_{ilk} belonging to the excluded sheets of the same group are present in each of the parts. Such a line is drawn for all of the sheets of the pack B_{ilk}.

These lines must be curves of the same radius whose centers lie on the output scale S_V. We therefore replace them with curves of approximately the same radius drawn by hand. At this, of course, it is necessary to violate the reticularity of the formative functions. Therefore, the division of the points E_{ilk} of each of the curves into three groups will not correspond precisely to the division of the corresponding sheets into packs.

With the help of the transparent gage with concentric curves the center of the curve drawn by hand is found. This center is marked on the curve. By doing this same thing with the remaining packs B_{ijk} (j = const) we get five different curves for the scale S_V, which serve as the basis for the selection of the best position of the output scale S_V.

Finally, when we know the radius and the position of the curve of the scale S_V as well as the field E_{ijk}, we can derive the graduation of the output scale.

4.10 Further Procedure of the Formulation. We have obtained new, more precise basis for the formulation of the parameters for the drawing of the color curve tentatively selected in the beginning. With the help of this new basis we again draw the color curve and repeat the whole process from the beginning until we are satisfied with the result, i.e., until we are no longer able to improve the parameters of the mechanism.

In this way we have found the parameters of the mechanism which forms the function $f(x_1, x_2, x_3) = x_4$ with precision, which, until the search is more successful, is sufficient to enable improvement of the mechanism with the help of suitable numerical methods.

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5. Ten-Joint Mechanism as Nomogram

5.1 Precision of Mechanism after First Formulation. Example. The ten-joint mechanism can be represented by the nomogram shown in Fig.8. The scales of this nomogram correspond to the scales S_I, S_J, S_K, S_V of the mechanism, and are drawn on the nomogram on curves whose radii correspond to the lengths of the cranks. On the transparent gage of the nomogram two pairs of curves are drawn. The curves of both pairs are concentric. The clearance between centers of these pairs corresponds to the length of the central draw-rod TS. The radii of the first pair of concentric curves correspond to the lengths of the draw-rods T_I and T_J, the radii of the second pair to the lengths of the draw-rods T_K and T_V. Each of the curves on the transparent gage has its own scale. By the intersections of the curves of the transparent gage and their respective scales of the nomogram the values of the corresponding variables are determined. The construction of the values of the independent variables is best accomplished by constructing the values of the independent variables x_i and x_j in the form of intersections of the scales S_I and S_J with the corresponding curves of the first pair of concentric curves of the transparent gage. In the center of these curves of the transparent gage, by holding and rotating it, we construct the corresponding curves of the second according to the selected value of x_k on the scale S_K. The intersection of the second curve of this pair with the output scale determines the functional value of the depicted function.

Figure 10 shows a nomogram which depicts the same function as the nomogram of Fig.9. The nomogram of Fig.9 was selected at random. The function depicted by it was selected for the given function for which th[illegible]s to be designed the mechanism which would depict it. The functional scales of the nomogram of Fig.9 were denoted as follows: the two input scales belonging to the same pair of concentric curves were denoted scales S_I and S_K of the variables x_i and x_k. The scales lying on the other side of the central draw-rod were denoted scales S_J and S_V of the variables x_j and x_v. Therefore, for finding the mechanism the requirement arose

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that on the one side of the central draw-rod must lie the scales of the variables x_i and x_j and on the other side the scales of the variables x_k and x_v. This makes it necessary to find equivalent mechanisms which have alternately two scales lying on different sides of the draw-rod. Figure 10 shows the nomogram corresponding to the formulation of such a mechanism in the stage of synthesis after the end of the first step, i.e., after one application of the procedure described in paragraph 4.2. This is, therefore, in the stage of the first formulation. The synthesis was not continued further because it was only carried out for the purpose of the verifying of the method of formulation. The method of solution finally adopted was somewhat different, because at the time that the method was worked out the described method of arranging the field of points D_{ij} was not yet known.

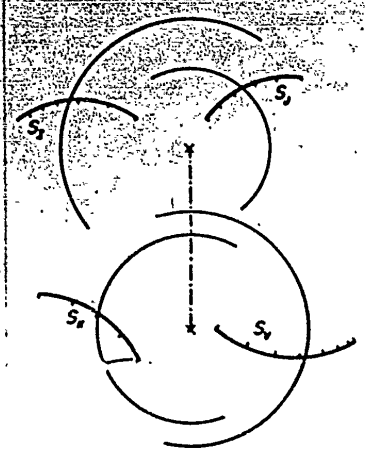

Fig.8 - Nomogram representing Ten-Joint Mechanism with Three Degrees of Freedom. The scales of the variables lie on the curves. Two pairs of concentric curves (extended thin) are drawn on the transparent gage

For judging the precision of the depiction of the selected function by this first approximation of the formulated mechanism, we present the Tables of Fig.11. The Table of Fig.11a gives some of the functional values of the function depicted by the nomogram of Fig.9, the Table of Fig.11b the functional values of the same points of the network of the functions depicted by the nomogram of Fig.10. The values of the points of the network (5, 5, 5) are included only for the sake of completeness. These are the values lying at the ends of the scales, i.e., in

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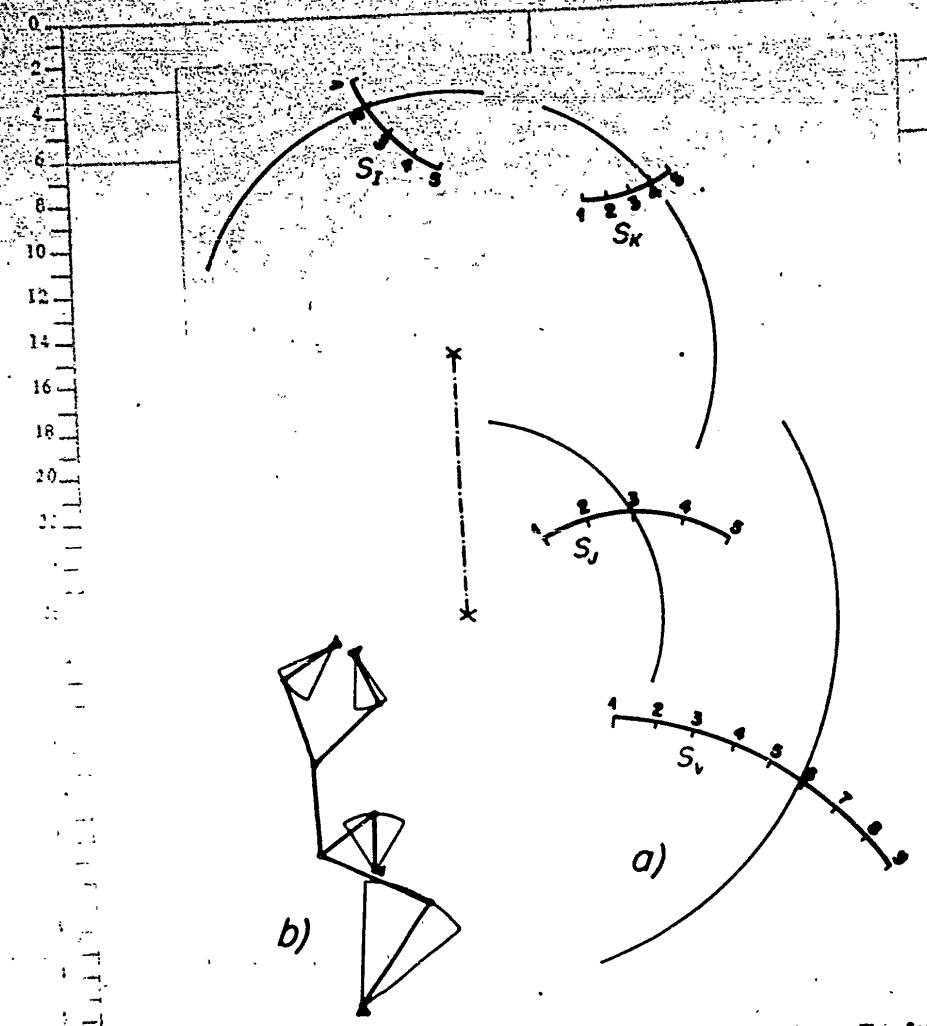

Fig.9 - Nomogram Representing Randomly-Selected Mechanism. The formative function of this mechanism was selected as the given function for which a mechanism which would depict it had to be found

a) Nomogram; b) Appearance of corresponding mechanism

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regions to which only the most necessary attention is devoted at the first step of the formulation.

Remarks: The method of formulation of ten-joint mechanism was worked out in

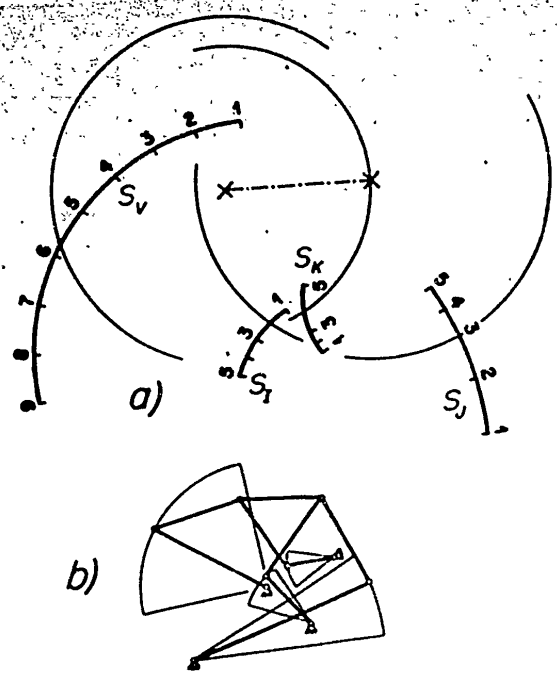

Fig.10 - Nomogram Representing Mechanism Equivalent of Mechanism of Fig.9 in State of Synthesis after End of First Step. The scales S_J and S_K are interchanged compared with Fig.9

a) Nomogram; b) Appearance of corresponding mechanism

the autumn of 1949, when the example in paragraph 5.1 was also worked out. It was published for the first time in the autumn of 1951 by the Central Institute of Mathematics, Department of Machines for Processing Information. For the sake of completeness it should be added that paragraphs 3.8 and 4.7 are parts of a 1953 seminary work to the Laboratory of Mathematical Machines.

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The problem of the synthesis of joint mechanisms with one degree of freedom was solved during the Second World War by A.Svoboda, who gave two methods for the

i	k	j=5	j=4	j=3	j=2	j=1
1	1	6,1	5,8	5,2	4,3	3,2
3	3	7,8	7,4	6,7	5,5	3,8
5	5	9	8,5	7,5	5,2	2,8
2	4	7,3	6,7	5,8	4,7	3,2
4	2	8,5	8	7,4	6,2	4,6

a

i	k	j=5	j=4	j=3	j=2	j=1
1	1	6,2	5,7	5,1	4,2	3,2
3	3	8	7,4	6,6	5,5	3,8
5	5	9,7	8,7	7,4	5,2	2,7
2	4	7,4	6,7	5,8	4,7	3,1
4	2	8,8	8,2	7,4	6,2	4,4

b

Fig.11 - a) Table of Formative Functions of Mechanism of Fig.9. b) Table of Formative Functions of Equivalent Mechanism of Fig.10 in Stage of Synthesis after End of First Step

solution of four-joint mechanisms. Moreover, a method was described in 1948 for the synthesis of joint mechanisms with two degrees of freedom. There is introduced here the concept of the grid structure of functions with two independent variables, which was not in the cited works extended to functions with several independent variables.

The concept of the network structure might easily be confused with the concept of the grid structure used by A.Svoboda in the work on which this work is based (Bibl.1). It should be noted that despite the confusing similarity of the concepts, there is no known connection between them.

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SUMMARY

Several methods of mechanically generating functions of two independent variables are known, e.g., the use of three-dimensional cams or linkage mechanisms of

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two degrees of freedom [1]. Hitherto no method for mechanically generating a given function of three variables has been known. In this preliminary announcement, a graphical method of synthesizing a mechanism with ten joints of three degrees of freedom is described, applicable to functions of quite a general class. The method is based on the new concept - the net structure of a function - which is the center of interest of the present article.

The introductory chapter discusses the design of linkage mechanisms generally. In Chaps.2 and 3 the concept of the net-structure of a mechanism is defined and the concepts necessary for its synthesis are introduced. Chap.4 describes the method of synthesis. In Chap.5 an example of such a mechanism is described.

The concept of the net-structure of a function, defined in the present work, is not to be confused with the concept of the grid-structure of a function introduced in the work of A.Svoboda, on which the present study is based.

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MULTIPOLES FOR ADDITION OF ELECTRICAL VOLTAGES COMPOSED OF OHMIC RESISTANCES*

by

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Received: 13 November, 1953

1. Introduction

In electrical analogous calculating machines the following problem is encountered:

From several input voltages (u_1 to u_n) we have the form one or more output voltages (v_I to v_N) in such a way that the output voltage is a linear combination of the input voltages:

$$v_x = p_{x1}u_1 + p_{x2}u_2 + \dots + p_{xn}u_n . \qquad (1)$$

This operation is solved in the majority of electrical analogous calculators by using summed multipoles according to Fig.1. The input terminal is connected via a resistance element with the output terminal (0), at which a loading resistance(r_o) is connected. The output voltage is given by the expression

$$v_0 = \sum_{k=1}^{n} \frac{v_k}{r_k} R \quad \text{where} \quad R = \frac{1}{\sum_{k=0}^{n} \frac{1}{r_k}} \qquad (2)$$

For comparison with eq.(1) therefore

$$p_{0k} = \frac{R}{r_k} .$$

If several output voltages are required, several summing multipoles of this type are used. The input resistance of such a multipole is not constant but de-

* Presented to the Second Regular Conference of the Laboratory of Mathematical Machines of the Czechoslovakian Academy of Sciences in December 1953.

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pends on the value of the output voltage (e_o). (The current i_k is proportional with the value $e_k - e_o$.) In order to use summand multipoles of the described type, it is necessary to fulfill the following conditions:

1. The internal resistances of the electromotive forces e_1 to e_n are negligibly small compared with the resistances r_1 to r_n;

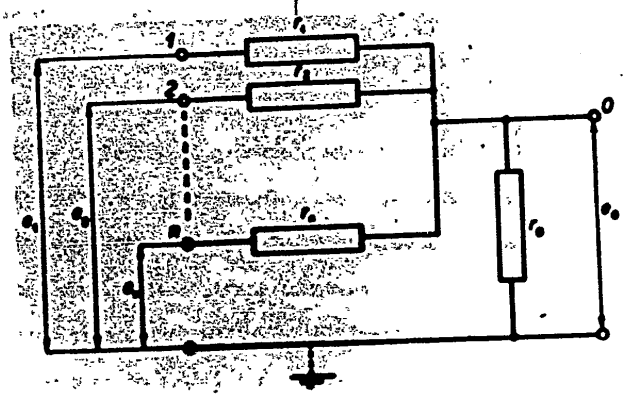

Fig.1 - Summing of Multipoles

2. All of the coefficients in eq.(1) are positive;

3. The loading resistance (r_o) is constant. It is undesirable for the coefficient P_{k1} to be very small and it may not be negligibly small compared with the resistance r_k;

4. If only one output voltage is required (one linear combination of the input voltages) it is only necessary for the internal resistance of the input electromotive force to be constant in order to be included in the resistance r_k.

From conditions 1 and 2 it follows that it is necessary for the internal resistance of the input branches to be negligibly small compared with the resistance of the loading resistance (r_o) or compared with the input resistance of the branches connected at the output terminals of the multipoles. If, therefore, there is only one output voltage (condition 4), it is usually more advantageous to transform the

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internal resistance of the input branches to a very small value (for example, with electronic amplifiers) than to solve the branches in such a way as always to have a constant internal resistance. Therefore the described characteristics of the mentioned multipoles are not disadvantageous when amplifiers with a negligibly small internal resistance compared with the input resistance are used in the arrangement. If it is not desired to employ such amplifiers the summation of the multipoles according to Fig.1 is not suitable, and especially not when the calculation of the branches is fairly complicated.

It is possible to construct a 2n-pole with a purely ohmic resistance which has a constant input resistance (for example, the same) with the loading resistance. Then it is possible to connect such a 2n-pole directly between the branches of the calculator without amplifiers or transformation of the impedances. The disadvantages of such 2n-poles compared with the multipoles according to Fig.1 are:

1. The voltage must be calculated symmetrical with the given (zero) potential if the employment of a transformer is to be avoided;

2. The calculation of the internal connections of the 2n-poles is more complicated.

On the other hand, they have the following further advantages:

1. The coefficient p_{kl} in eq.(1) may be positive or negative;

2. They can be constructed for any number of pairs of output terminals.

The matrix equations for the calculation of the internal connections of 2n-poles of the latter type were derived by Dr.Fischer in 1938 (Bibl.1). The derivation was carried out for the special case where each pair of terminals works with a particular preselected characteristic (wave) resistance. It is therefore assumed that the internal resistance of the output terminals of the 2n-pole is in agreement with the loading resistance at the same pair of terminals if the internal resistance of the branches feeding the input terminals of the 2n-pole is in agreement with the input resistance of the corresponding pair of input terminals. Therefore the calcu-

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lating 2n-poles are also used for the summation of the voltages in the proposed electrical analog computers (2, 3).

The assumptions made by Dr. Fischer are unfulfilled in every case coming under observation in the practice. The author has in part 3.2 derived the matrix relations for the calculation of the internal structure of 2n-poles with which a particular, preselected internal resistance of the output terminals, generally different from the corresponding loading resistance can be required. The internal resistance of the input branches may likewise by any preselected one different from the input resistance of the 2n-pole.

Usually a particular value of the internal resistance of the output terminals of the 2n-pole is not required at all. For this case the author has derived in part 3.1 directly-employable equations for calculating the internal connections. The author has derived these equations for the requirement that the action of the 2n-pole be as great as possible and the internal connections as simple as possible. For this case it is still possible to use the equations used by Dr. Fischer. Compared with the latter, however, the formulas derived by the author have the following advantages:

1. They enable putting in higher values of the coefficient p_{kl};

2. They are simpler, especially when the 2n-pole has a large number of pairs of output terminals;

3. At the employment of a purely ohmic resistance in the form of a 2-pole composed of 2n-poles it is possible to write directly-employable, relatively-simple formulas for the values of this 2-pole;

4. The internal connections of the 2n-poles are somewhat simpler.

For the sake of simplicity the author derives the relations only for the ohmic value of the resistance and the real value of the coefficient p_{kl}. The method for determining the conductivity of the matrix (Y) of the 2n-pole is wholly different from the method employed by Dr. Fischer.

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In part 4 the author has derived the formulas and method of calculation of the required precision of the resistance elements of the 2n-pole according to the metho of Bychovskii (Bibl.4).

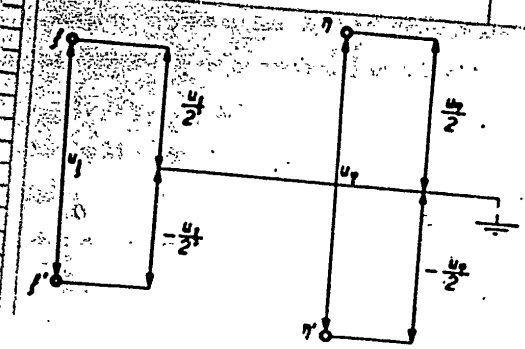

Fig.2 - The Definition of Symmetrical Voltage

2. Assumptions and Denotation

The voltage between the two terminals ξ and ξ' (Fig.2) is called symmetrical if the terminal ξ has compared with zero potential a potential of the same magnitude as the terminal ξ' but in the opposite direction. If the terminals are connected for symmetrical voltage, and the current flowing into the terminal ξ is of the same magnitude as the current flowing into the terminal ξ' but in the opposite direction, we call the two terminals symmetrically associated.

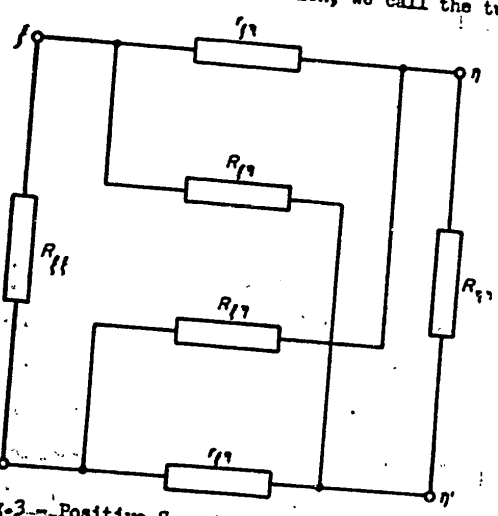

Fig.3 - Positive Symmetrical Four-Pole

If a multipole contains only one pair of symmetrically-associated terminals we call it a symmetrical 2n-pole. A symmetrical voltage is called positive if the potential of the terminal ξ is positive and the potential of the terminal ξ' is negative (Fig.2). The current between the terminals ξ and ξ' is denoted positive if it flows into the terminal ξ and flows out of the terminal ξ', and is denoted negative if it flows out of the

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terminal ξ and flows into the terminal ξ'.

The elements of a symmetrical 2n-pole are arranged symmetrically. The 2-pole $r_{\xi\eta}$ connected between the terminal ξ and η is in agreement with the 2-pole connected between the terminals ξ' and η', and the 2-pole $R_{\xi\eta}$ connected between the terminal η and η' is in agreement with the 2-pole connected between the terminals ξ and η, etc (Fig.3). All of the terminals provided with a prime ξ', η', etc., are called mutually same-lying, while the terminals not provided with a prime are called same-lying.

When we do not advance the internal connections of the 2n-pole, we assume that each of the terminals of the 2n-poles is connected via some 2-pole with each of the remaining terminals. A two-pole connected between same-lying terminals is denoted $r_{\xi\eta}$, i.e., with the index denoting a connected pair of terminals. A two-pole connecting a non-same-lying pair of terminals is denoted $R_{\xi\eta}$. For simplifying the expressions, we shall use the reciprocal values of these impedances, i.e., the admittance $g_{\xi\eta}$ connected between the same-lying terminals of the 2n-pole and the admittance $h_{\xi\eta}$ connected between the non-same-lying terminals:

$$g_{\xi\eta} = \frac{1}{r_{\xi\eta}}, \quad h_{\xi\eta} = \frac{1}{R_{\xi\eta}}. \tag{3}$$

We make the assumption that the 2n-pole can only be composed of passive 2-poles (special ohmic resistance) of unknown conductive connection with no limitation of the external characteristics, as mentioned by Dr. Fischer (Bibl.1). If the 2n-pole contains still other terminals in the connection, we can advantageously exclude star-triangle transformation. The assumption, of course, excludes employment of a transformer.

For expressing the external characters of the 2n-pole the conductivity mother Y is employed. The matrix exists at the assumed internal connections for all cases of practical employment (but not the resistance matrix). With the matrix Y it is likewise easy to determine the structure and value of the 2-poles forming the

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internal connections of the 2n-pole. The matrix Y expresses the relation between the current and the voltage on all of the pairs of associated terminals of the 2n-pole:

$$I = YU \tag{4}$$

or

$$U = Y^{-1} I \tag{5}$$

Determination of the internal connections of the 2n-pole from the matrix Y. The relation between the matrix Y and the conductivity of the 2-poles composing the 2n-pole was derived by Fischer:

$$y_{xy} = \tfrac{1}{2}(h_{xy} - g_{xy}) \tag{6}$$

$$y_{xx} = \tfrac{1}{2}\left[\sum_{k \neq x}^{n} h_{xy} + \sum_{k \neq x}^{n} g_{xy}\right] + h_{xx} \tag{7}$$

The relation is easily ascertained by imagining that all of the terminals are shortcircuited except one x, x', to which we apply the voltage u_x. Then the conductivity y_{kx} expresses the relation between the current of the corresponding pair of terminals k, k' and the voltage u_x. Because the conductivities (or the real parts of the admittances) g_{xy} and h_{xy} of passive 2-poles cannot be negative the following condition is valid

$$\operatorname{Re} y_{xx} \geq \sum_{k \neq x}^{n} |\operatorname{Re} y_{xk}| \tag{8}$$

and of course

$$y_{kl} = y_{lk}, \tag{9}$$

in order for the matrix Y to be realized with the passive 2-poles.

The matrices Y are determined for all of the (external) characteristics of the 2n-pole. From eq.(6) and (7) it can be seen that the individual 2-poles are not matrices Y, so that neither can the external characteristics of the 2n-pole be un-

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ambiguously determined. However, we can always select one of the conductivities g_{xy} or h_{xy} at zero. Then we have*

$$g_{xx} = -2y_{xx},\ h_{xx} = 0, \quad \text{if} \quad y_{xx} < 0$$
$$g_{xx} = 0, \quad h_{xx} = 2y_{xx}, \quad \text{if} \quad y_{xx} > 0 \tag{10}$$

and

$$h_{xx} = y_{xx} - \sum_{x \neq x}^{n} |y_{xx}|$$

3. Methods for Determining Matrix Y

For making the solution more legible, we shall denote the input terminal with a small letter, the output terminal with a large letter, in the matrix denote the value at the input terminal with one prime, the value on the output terminal with two primes. The voltages put in at the terminals of the 2n-pole we denote with the letters u, U, the voltages measured at the loading terminals of the 2n-pole with the letters v, V.

Equation (1) is then expressed in the form of:

$$V'' = PU'. \tag{11}$$

The matrix of the output voltage v" is one-columnar with N terms, the transmission matrix P is a rectangle with n columns and N lines, the matrix of the output voltage U' is one-columnar with n terms. The loading resistance of the output terminal is denoted z_K.

We have then the matrix relations:

$$V'' = -Z''I'' \quad \text{or} \quad I'' = -Z''^{-1}V''. \tag{12}$$

The resistance of the input terminal is denoted w_K and the matrix relations:

---

* When the admittances y_{yx}, g_{yx} and h_{yx} are complex, eqs.(10) are valid for the real part of the admittances. The imaginary parts of the conductance y_{xy} can be distributed arbitrarily between the admittances g_{yx} and h_{yx}.

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$$U' = W'I' \quad \text{or} \quad I' = W'^{-1}U'. \tag{13}$$

The matrices of the input and loading resistances are diagonal.

The matrix W' has n terms, the matrix Z" has N terms.

The matrix of the internal resistance of the output terminal W" (diagonal with N terms) gives us the relation between the voltage conducted to the output terminal u_k and the current in the output terminal:

$$U'' = W''I'' \quad \text{or} \quad I'' = W''^{-1}U''. \tag{14}$$

The matrix of the internal resistance of the output terminal W" is a diagonal with N terms.

For determining the internal resistance of the output terminal we must know the internal resistance of the ems fed to the input terminal z_k, and hence the relation

$$V' = -Z'I' \quad \text{or} \quad I' = -Z'^{-1}V' \tag{15}$$

and the matrix of the return transmission from the output to the input terminal

$$V' = P'U'. \tag{16}$$

The matrix Z' is a diagonal with n terms and the matrix P' is a rectangle with N columns and n lines.

Further, we divide the matrix Y into four submatrices:

$$Y = \begin{vmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{vmatrix}. \tag{17}$$

The submatrix Y_1 is therefore a square with n lines and columns, and corresponds to the conductivity connected between the input terminals (except for the diagonal terms).

The submatrix Y_4 is a square with N lines and columns, and corresponds to the conductivity connected between the output terminals (except the diagonal terms).

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The submatrix Y_2 is a rectangle with n columns and N lines, and corresponds to the conductivity connected between the input and the output terminals.

The submatrix Y_3 is a rectangle with N columns and n lines. According to eq.(9) the following is valid:

$$Y_2 = \bar{Y}_3 \text{ and } Y_3 = \bar{Y}_2 . \tag{9a}$$

(The stroke denoted the transported matrix.)

Then eq.(4) is re-written as follows:

$$\begin{vmatrix} I' \\ I'' \end{vmatrix} \begin{vmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{vmatrix} \begin{vmatrix} U' \\ V'' \end{vmatrix}. \tag{18}$$

We represent the internal resistance of the output terminal as follows:

$$\begin{vmatrix} I' \\ I'' \end{vmatrix} = \begin{vmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{vmatrix} \begin{vmatrix} V' \\ U'' \end{vmatrix}. \tag{18a}$$

With eqs. (11) to (18) we suitably express all of the relations determining the external characteristics of the 2n-pole. Next we exclude from the equation the values of the current (I', I'') and of the voltages (U', U'', V', V''), obtain the relation between Y and the transmission matrix P, and with the matrices determine the resistance characteristics of the 2n-pole (Z', W' and Z'', W'').

We must always determine the matrix of the transmission coefficient P and of the loading resistance Z''. However, we need not always determine the internal resistance of the output terminals, i.e., we do not know either the matrix W'' or the internal resistance of the source feeding the input terminal Z'.

Of course, the unknown matrices could be selected arbitrarily, but an unsuitable selection of these matrices would considerably lower the action of the 2n-pole, i.e., the maximal magnitude of the coefficient of transmission p_{Kl}.

The problem of formulating a summing 2n-pole usually consists in having the level of the output voltage as high as possible and hence the transmission p_{Kl} as great as possible. It is clear that the action of a 2n-pole will be greater the

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smaller is the resistance (the greater is the conductance) which is connected between the input and output terminals. The magnitude of the conductance y_{xy} is limited by the inequality (8) which must be fulfilled for all of the pairs of terminals. If, therefore, we attain the maximal action of the 2n-pole, equality will be attained in eq.(8) for (at least) one of the pairs of terminals.

If we have not determined for the 2n-pole all of the resistance characteristics, we can suitably select directly some terms of the matrix Y in such a way that the maximal magnitude of the coefficient of transmission is not limited and that the greatest conductance is zero.

Let us investigate two cases:

1. We know the loading resistance of the output terminals (the matrix Z"), and it is required that, at the prescribed transmission characteristic of the 2n-pole, the input resistance of the 2n-pole be constant and preselected.

2. It is required of the output terminal that it have a constant, preselected internal resistance. Then, of course, the internal resistance of the branch feeding the input terminals must likewise be constant (the matrix Z'). The remaining characteristics must be the same as in case 1.

3.1 Summation of 2n-Pole with Constant Input Resistance. Of the summing 2n-pole it is required that the output voltage be given by the linear combination of the input voltages and that the input resistance at the input terminals of the 2n-pole have a constant value when the output is loaded with the given loading resistance. From eqs.(11), (12), and (13) we get

$$\begin{aligned} W'^{-1} &= Y_1 + Y_2 P \\ Z'^{-1} P &= Y_3 + Y_4 P \\ (Y_2 &= \bar{Y}_3). \end{aligned} \tag{19}$$

For the four matrices we have only three relations. We can select the submatrix Y_4 as a diagonal; the diagonal term of the submatrix Y_4 cannot be selected zero because of eq.(8). From the arranged eq.(19)

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$$\begin{aligned} Y_3 &= -(Z^{-1} + Y_4)P \\ Y_1 &= W^{-1} - Y_3 P \end{aligned} \tag{20}$$

we can then directly write the terms of the matrix Y

$$\begin{aligned} y_{kl} &= -\left(\frac{1}{z_k} + y_{kk}\right) p_{kl} \\ y_{kl} &= -\sum_{k=1}^{r} y_{kk} p_{kl} \\ y_{kk} &= \frac{1}{w_k} - \sum_{k=1}^{r} y_{kk} p_{kk} \end{aligned} \tag{21}$$

and

Moreover, we can select

$$y_{kk} = \sum_{k=1}^{n} |y_{kk}| \tag{22}$$

Finally, we get the formulas for the terms of the matrix Y

$$\begin{aligned} y_{kl} &= -p_{kl} \frac{1}{z_k\left(1 - \sum_{k=1}^{n} |p_{kk}|\right)} \\ y_{kl} &= \sum_{k=1}^{r} \frac{p_{kk} p_{kl}}{z_k\left(1 - \sum_{k=1}^{n} |p_{kk}|\right)} \\ y_{kk} &= \frac{\sum_{k=1}^{n} |p_{kk}|}{z_k\left(1 - \sum_{k=1}^{n} |p_{kk}|\right)} \\ y_{kk} &= \frac{1}{w_k} + \sum_{k=1}^{r} \frac{p_{kk}}{z_k\left(1 - \sum_{k=1}^{n} |p_{kk}|\right)} \\ y_{kl} &= 0 \quad \text{for} \quad K \neq L. \end{aligned} \tag{23}$$

The magnitude of the coefficient p_{Kl} limits eq.(8). The maximal value of the coefficient of transmission is obtained when at least one of the pairs of input terminals satisfies the equation

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$$y_{ii} = \sum_{i \neq k}^{n} |y_{ki}| + \sum_{k \neq i}^{n} |y_{ik}| \tag{24}$$

The internal connections of this 2n-pole are as follows: All of the pairs of output terminals are connected via resistance elements with all of the pairs of input terminals, all of the pairs of input terminals are connected with each other via resistance elements. The pairs of input terminals are over-arched by resistance elements. If the maximal coefficient of transmission is employed, at least one of the pairs of input terminals is not over-arched by a resistance element. If it is advantageous, for example, because of a more advantageous value of the resistance elements (of the 2n-pole), further terminals can be brought into internal connection for suitable triangle-star transformation.

Example: We have to determine the internal connections of a 2n-pole which has two pairs of input terminals 1, 1' and 2, 2', and one pair of output terminals I, I'. The input resistance of the two input terminals has to be the same and equal to the loading resistance of the output terminal z. The transmission coefficient from both input terminals to the output terminal must be the same and maximal.

In eq.(23) we put:

$$w_1 = z,\ w_2 = z,\ z_1 = z,$$
$$p_{11} = p_{21} = p$$

We get:

$$y_{11} = -p\frac{1}{z(1-2p)}$$
$$y_{21} = -p\frac{1}{z(1-2p)}$$
$$y_{12} = p^2\frac{1}{z(1-2p)} \tag{23a}$$
$$y_{11} = p\frac{1}{z(1-2p)}$$

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$$y_{11} = y_{22} = \frac{1}{z} \cdot \frac{p^2}{1-2p}.$$

In order for the coefficient of transmission to be maximal, eq.(24) must be fulfilled for one of the pairs of input terminals, so that

$$y_{11} = |y_{12}| + |y_{21}|$$

or

$$y_{22} = |y_{12}| + |y_{21}|.$$

The condition is valid giving the smaller value of the coefficient of transmission. In our case both conditions are the same. The equation

$$\frac{1}{z}\left(1 + \frac{p^2}{1-2p}\right) = \frac{1}{z}\left(\frac{p^2}{1-2p} + \frac{p}{1-2p}\right)$$

gives the solution $p = \frac{1}{3}$.

We put the value $p = \frac{1}{3}$ in eq.(23a) and get

$$y_{12} = y_{21} = -\frac{1}{z}$$

$$y_{22} = \frac{1}{3}\frac{1}{z}$$

$$y_{11} = \frac{1}{z}$$

$$y_{11} = y_{22} = \frac{4}{3}\frac{1}{z}$$

From eq.(10) we have then

$$g_{11} = g_{22} = \frac{2}{z}, \quad r_{11} = r_{22} = \frac{z}{2}$$

and

$$h_{12} = \frac{2}{3}\frac{1}{z}, \quad R_{12} = \frac{3}{2}z$$

$$h_{11} = h_{22} = 0.$$

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The required internal connections of the 2n-pole can be seen from Fig.4.

3.2 Summation of 2n-Pole with Constant Input, Preselected Resistance and Constant, Preselected Internal Resistance. Of the summing 2n-pole it is required that:

The output voltage be the linear combination of the input voltages;

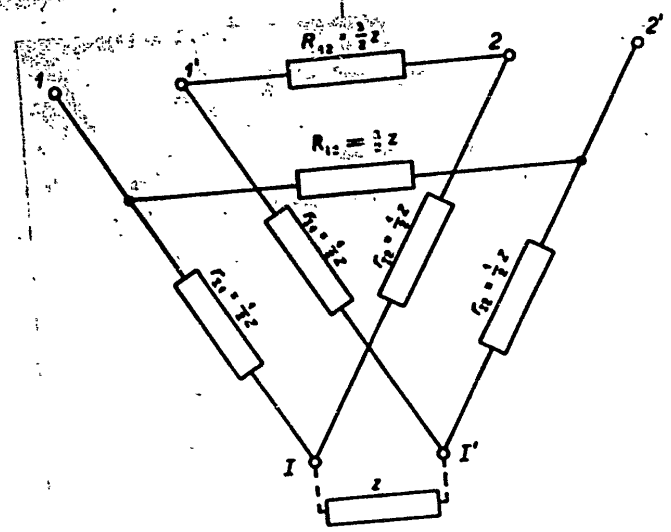

Fig.4 - Scheme of Connections of 2n-Pole of Example 3.1

The input resistance at the input terminals be a definite constant value at the output resistance loaded with the given loading resistance;

That the internal resistance of the output terminal have a definite constant value when the source feeding the input terminals has a given constant internal resistance. From conditions (11) to (16) we get the relations

$$\begin{aligned} Y_1 + Y_2 P &= W'^{-1} \\ Y_3 + Y_4 P &= -Z'^{-1} P \\ Y_1 P' + Y_2 &= -Z'^{-1} P' \\ Y_3 P' + Y_4 &= W'^{-1} . \end{aligned} \qquad (25)$$

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From these relations we ascertain the individual parts of the matrix Y:

$$Y_1 - W'^{-1} - Y_2 P = W'^{-1} + (Z'^{-1} + W'^{-1}) P' (J - PP')^{-1} P \tag{26}$$

$$Y_2 = -(W'^{-1} + Z'^{-1}) P' (J - PP')^{-1}$$

$$Y_3 = -(Z'^{-1} + W'^{-1}) (J - PP')^{-1} P$$

$$Y_4 = (W'^{-1} + Z'^{-1} PP') (J - PP')^{-1}.$$

From the condition $Y_2 = \bar{Y}_3$ we determine the matrix of the return conductance:

$$P' = \bar{P}(W'^{-1} + Z'^{-1})(W'^{-1} + Z'^{-1})^{-1}. \tag{27}$$

The maximal magnitudes of the terms of the matrix P are again limited by eq.(8). For reaching the maximal action of a summing 2n-pole of this type, for at least one of the pairs of terminals (input or output) the condition must be satisfied

$$y_{ii} = \sum_{m+1}^{n} |y_{im}| + \sum_{N+1}^{N} |y_{in}|. \tag{28}$$

The internal connections of the 2n-pole of the latter type are as follows: All of the pairs of input and output terminals are connected with each other via resistance elements. All of the pairs of terminals are over-arched by resistance elements. If the maximal value of the coefficient of transmission is employed, at least one of the pairs of terminals (input or output) is not over-arched by a resistance element.

It is required that the internal resistance of the output terminal be the same as the loading resistance and that the internal resistance of the source feeding the input terminals be the same as the corresponding input resistance of the 2n-pole (at which all of the pairs have the characteristic, wave resistance), at which the following are valid

$$W' = Z' \text{ and } W'' = Z''.$$

The parts of the matrix Y will then be:

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$$
\begin{aligned}
Y_1 &= Z^{-1} - Y_2 P \\
Y_2 &= \bar{Y}_3 \\
Y_3 &= -2Z^{*-1}(J - PZ^{*}Z^{*-1}P)^{-1}\bar{P} \\
Y_4 &= Z^{*-1}(J + PZ^{*}Z^{*-1})(J - PZ^{*}Z^{*-1}\bar{P})^{-1}
\end{aligned}
\tag{29}
$$

If the 2n-pole has only one pair of output terminals (0, 0'), then

$$
(J - PZ^{*}Z^{*-1} - \bar{P})^{-1} = \frac{1}{1 - \sum_{k=1}^{n} a_k p_{0k}^2}
\tag{30}
$$

and we write

$$
a_k = \frac{z_k}{z_0}.
$$

The individual terms of the matrix Y can then be expressed as follows:

$$
\begin{aligned}
y_{00} &= \frac{1}{Az_0}\left(1 + \sum_{k=1}^{n} a_k p_{0k}^2\right) \\
y_{km} &= \frac{1}{Az_0} \cdot 2p_{0k}p_{0m} \\
y_{k0} &= -\frac{1}{Az_0} \cdot 2p_{0k} \\
y_{mm} &= \frac{1}{Az_m}\left(1 - \sum_{k=1}^{n} a_k p_{0k}^2 + 2a_m p_{0m}^2\right)
\end{aligned}
\tag{31}
$$

where $A = 1 - \sum_{k=1}^{n} a_k p_{0k}^2$.

Prof. Fischer, at operating with wave resistance at all of the terminals, derived for the 2n-pole for the matrix Y the following relation:

$$
Y = Z^{-1}(2P^{-1} - J).
\tag{32}
$$

The matrix Z is formed by the wave resistances of all of the pairs of terminals (input and output), the matrix P contains the transmission coefficients in both directions in agreement with eq.(27):

$$
p_{kl} = \frac{z_l}{z_k} \cdot p_{lk}
\tag{33}
$$

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and the terms

$$p_{11} = p_{22} = 1, \; p_{01} = p_{02} = 0 \tag{34}$$

All of the matrices are squares with n plus N lines and columns.

Example: We have to determine the internal connections of a 2n-pole (six-pole) which has two pairs of input terminals 1, 1' and 2, 2', and one pair of output terminals (0, 0').

It is required that the input resistance of both input terminals be the same and equal to the loading resistance of the output terminals z. It is further required that the internal resistance of the output terminal be likewise equal to z when the internal resistances of the branches feeding the input terminals of the six-pole are likewise equal to the value z. The transmission coefficients of both input terminals must be the same and maximal.

In eq.(31) we put

$$z_0 = z_1 = z_2 = z, \; p_{01} = p_{02} = p \, .$$

We get

$$y_{00} = \frac{1 + 2p^2}{z(1 - p^2)} \qquad y_{12} = \frac{2p^2}{z(1 - p^2)}$$

$$y_{11} = y_{22} = \frac{1}{z(1 - p^2)} \qquad y_{01} = y_{02} = -\frac{2p}{z(1 - p^2)} \, .$$

In order for the coefficient of transmission to be maximal, eq.(28) must be satisfied so that

$$y_{00} = |y_{01}| + |y_{02}|$$

or

$$y_{11} = |y_{01}| + |y_{12}|$$

or

$$y_{22} = |y_{02}| + |y_{12}| \, .$$

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There is again the least calculated p.

Putting it in gives the quadratic equations:

$$2p^2 = 2p + 2p$$

or

$$1 = 2p + 2p^2$$

or

$$1 = 2p + 2p^2.$$

The smallest value is given by the first equation, and, specifically, $p = 1 - \frac{1}{2}\sqrt{2} = 0.29289$. Putting it in eq.(31a) gives

$$y_{00} = \frac{1}{z} \cdot \frac{4 - 2\sqrt{2}}{\sqrt{2} - \frac{1}{2}}$$

$$y_{01} = y_{02} = -\frac{1}{z} \frac{2 - \sqrt{2}}{\sqrt{2} - \frac{1}{2}}$$

$$y_{11} = y_{22} = \frac{1}{z} \frac{1}{\sqrt{2} - \frac{1}{2}}$$

$$y_{12} = \frac{1}{z} \frac{3 - 2\sqrt{2}}{\sqrt{2} - \frac{1}{2}}$$

According to eq.(10) therefore we have

$$g_{01} = g_{02} = -2y_{01} = -2y_{02} = \frac{1}{z} \frac{4 - 2\sqrt{2}}{\sqrt{2} - \frac{1}{2}} \; ; \quad r_{01} = r_{02} = 0{,}78033\, z$$

$$h_{12} = 2y_{12} = \frac{1}{z} \frac{6 - 4\sqrt{2}}{\sqrt{2} - \frac{1}{2}} \; ; \quad R_{12} = 2{,}66423\, z$$

$$h_{11} = h_{22} = y_{11} - |y_{01}| - |y_{12}| = \frac{1}{z} \frac{3\sqrt{2} - 4}{\sqrt{2} - \frac{1}{2}} \; ; \quad R_{11} = R_{22} = 3{,}76818\, z$$

The internal connections can be seen from Fig.5.

In this case, we obtain the same results when using the formulas of Dr.Fischer.

4. Transmission of Resistance Elements of 2n Poles

At the formulation of a 2n-pole it is necessary to determine the transmissions for which the individual resistance elements will have to be made. It is clear

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that an error in any of the resistance elements has as a result an error in the voltages at all of the terminals of the 2n-pole, and, on the other hand, that an error

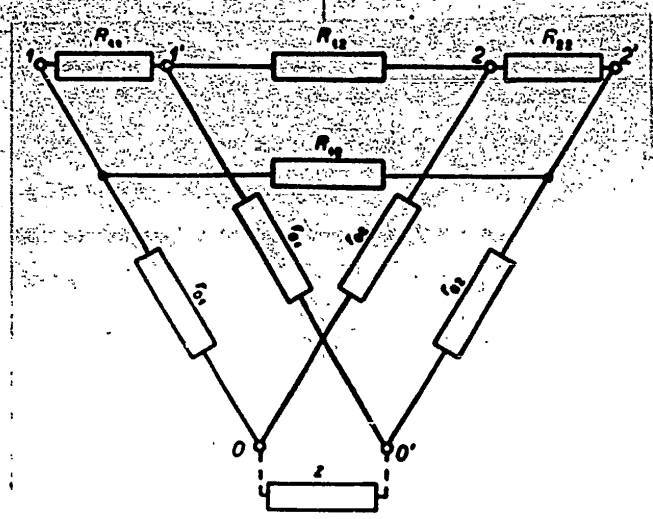

Fig.5 - Scheme of Connections of 2n-Pole of Example 3.2

in all of the resistance elements has an influence on the precision of any of the voltages. The error in the resistance element connected between two pairs of terminals brings about the greatest error in voltage at these two pairs of terminals. The magnitude of this error is determined according to the theorem of Bychovskii (Bibl.4). The errors in the voltages of the remaining pairs of terminals occurs as if these erroneous voltages were conducted to both pairs of terminals of an ideally-precise 2n-pole, and hence multiplied by the corresponding coefficients of transmission. For the sake of simplicity it will be assumed that the errors in the two symmetrically-connected conductances are the same, so that the 2n-pole, also at errors in the resistance elements, retains its symmetrical characteristics.

Consider two pairs of terminals ξ, ξ' and η, η', between which are connected resistance elements of conductance $b_{\xi\eta}$. According to Bychovskii the ratio between

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the error in the conductance $b_{\xi\eta}$ and the error in the voltage u_ξ or u_η (referred to the voltage u_ξ conducted to the terminals ξ, ξ') is given by the sum of the two coefficients of transmission

$$\frac{\partial u_\eta}{u_\xi} = -p_{b\xi}\, p_{\xi\eta}\, \frac{\partial b_{\xi\eta}}{b_{\xi\eta}}, \quad \frac{\partial u_\xi}{u_\xi} = -p_{b\xi}\, p_{\xi\xi}\, \frac{\partial b_{\xi\eta}}{b_{\xi\eta}} \tag{35}$$

The coefficient $p_{b\xi}$ denotes the ratio between the voltage in the resistance element of conductance $b_{\xi\eta}$ and the voltage conducted to the terminals $\xi\xi'$. The voltage in this resistance is the difference or the sum of the voltages in both pairs of elements

$$p_{b\xi} = \frac{u_\xi \mp u_\eta}{u_\xi} = 1 \mp p_{\eta\xi} \tag{36}$$

The minus sign applies to the conductance connected between same-lying terminals (conductance $g_{\xi\eta}$);

The + applies to the conductance connected between non-same-lying terminals ($b_{\xi\eta}$).

The coefficient of transmission $p_{\xi bs}$ or $p_{\xi bs}$ denotes the ratio between the voltage in the terminals η, η' or ξ, ξ' and the voltage connected in series with the conductance $b_{\xi\eta}$. Here all of the sources of electromotive force are shortcircuited. For determining these coefficients, we convert the whole 2n-pole into a four-pole connected between the terminals ξ, ξ' and η, η'. Since we assume that the 2n-pole has stable symmetrical characteristics, we can imagine the centers of all of the resistance connected between mutually-associated, grounded and mutually-connected terminals. The star connection formed in this way is converted into a star-triangle transformation similar to the scheme of connection represented in Fig.3. Therefore the conductance connected between the individual terminals includes all of the conductances of the 2n-pole including the loading resistance of the output terminals, including the internal resistance of the source feeding the input terminals, and including the considered erroneous conductance $b_{\xi\eta}$. We denote these substituted

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conductances with a cross (+). The solution of the connections gives the following coefficients of transmission:

$$p_{\eta\delta s} = b_{\xi\eta} \frac{h^{+}_{\xi\eta} + h^{+}_{\xi\xi}}{(h^{+}_{\xi\eta} + h^{+}_{\eta\eta})(g^{+}_{\xi\eta} + h^{+}_{\xi\xi}) + (h^{+}_{\xi\eta} + h^{+}_{\xi\xi})(g^{+}_{\xi\eta} + h^{+}_{\eta\eta})} \qquad (37)$$

$$p_{\xi\delta s} = b_{\xi\eta} \frac{h^{+}_{\xi\eta} + h^{+}_{\eta\eta}}{(h^{+}_{\xi\eta} + h^{+}_{\eta\eta})(g^{+}_{\xi\eta} + h^{+}_{\xi\xi}) + (h^{+}_{\xi\eta} + h^{+}_{\xi\xi})(g^{+}_{\xi\eta} + h^{+}_{\eta\eta})}$$

Summary

The authors give a method and the formulas for the calculation of multipoles used for the summation of electrical voltages. The multipole has a constant preselected input resistance or a constant preselected internal resistance. Its internal structure is similar to that of the 2n-pole proposed by Dr.Fischer (Bibl.1). The method of the author, however, enables the solution of this multipole for much more general requirements with respect to its characteristics.

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SUMMARY

Dr. Fischer proposed in his paper [1] 2n-poles composed solely of ohmic resistances, suitable for the summing of voltages. The author gives a new method of design of 2n-poles of similar structure, but of better efficiency and wider applicability.

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